IAIK Open Flow

Digital System Design SS25

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SCIENCE PASSION TECHNOLOGY



Introduction to Our Open Source Digital Design Flow

Outline

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Motivation

With the recent release of open source Process Design Kits (PDKs) such as SKY130 and advances in open source EDA tools, it is now possible to design manufacturable chips without the need to sign NDAs.

This document shows how to use the IAIK Open Flow to develop, test and integrate your cipher into a chip.

The goal is to provide students with the tools and framework to develop their cipher locally on their own computer.

SKY130 Stackup



Open Flow ASIC

- Acts as a harness for your cipher
- SoC with Ibex RISC-V Core
 - 8 kB ROM
 - 8 kB SRAM
- Various peripherals
- Repository: open-flow-asic



Open Flow Docker

- Container with open source tools
- Make sure to install docker
- List of tools: open-flow-docker
- Pull the image via:



\$ docker pull \
extgit.isec.tugraz.at:8443/sesys/iaik-open-flow/open-flow-docker

Open Flow Template

- Your working template for the DSD course
- Tasks are split into
 - ex1/ Files for exercise 1: cipher_core
 - ex2/ Files for exercise 2: cipher_peripheral
 - open-flow/tapeout/ Integration into harness
- Repository: open-flow-template

General Procedure

- The Open Flow ASIC has already been pre-hardened
- For now, a placeholder-macro is used instead of your cipher
 - Your goal: Create your cipher in 1000x1000 um
 - Communicate with the SoC over bus interfaces
 - Harden your cipher as a hard macro
 - Replace the empty wrapper in the final tapeout step
- This solution was chosen so that development of your cipher is possible on lightweight hardware such as laptops



Cipher Core - Sources

- All source files under ex1/
 - ex1/src/ RTL files
 - ex1/tb/ testbench
 - open-flow/ex1_aux/config.json
 config for OL2
 - open-flow/ex1_aux/pins.cfg
 pin config for OL2



Cipher Core - Output

- Output directories
 - ex1/runs/ OL2 output files
 - results/ex1_openlane/
 Most recent OL2 output
 - ex1/tb/sim_build/
 Simulation output

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Make Targets

- ex1-lint
- ex1-openlane
- ex1-openroad
- ex1-klayout
- ex1-cocotb
- ex1-cocotb-gl

To add additional source files to your cipher, just add them! All files ending in .sv are automatically picked up for the implementation and the simulation.

ex1/src/*.sv



Cipher Peripheral - Sources

- All source files under ex2/
 - ex2/src/ RTL files
 - ex2/tb/ testbench
 - ex2/sw/ software for the ibex core
 - open-flow/ex2_aux/config.json
 config for OL2



Cipher Peripheral - Output

- Output directories
 - ex2/runs/ OL2 output files
 - results/ex2_openlane/
 Most recent OL2 output
 - ex2/tb/sim_build/
 Simulation output



Make Targets

- ex2-lint
- ex2-openlane
- ex2-openroad
- ex2-klayout
- ex2-cocotb
- ex2-cocotb-gl

To add additional source files to your cipher, just add them! All files ending in .sv are automatically picked up for the implementation and the simulation.

ex2/src/*.sv



Tapeout Final Step

To complete the tapeout:

- Harden your cipher_peripheral
- Generate the ROMs for your program
- (Optionally) Update the chip art
- open-flow/tapeout/chip_art/chip_art.png



Tapeout

Make Targets

- tapeout-chip_art generate the layout for your chip art
- tapeout-rom generate the two ROM macros
 - Set \$PROGRAM env variable to active program
- tapeout-final perform the final merging of the layouts
 - Cipher, ROM and chip_art must be hardened
- tapeout-klayout open the final layout using KLayout

Tapeout

Set the active \$PROGRAM

- To change the program that is compiled, set the \$PROGRAM environment variable.
- Please note that you must create a folder with the same structure as the example program named ex2/sw/cipher-test.

This is necessary for:

- ex2-sw
- ex2-cocotb
- ex2-cocotb-gl
- tapeout-rom

Execute make targets like this:

\$ PROGRAM=cipher-test ex2-cocotb

General Makefile Targets

General Makefile Targets

\$ make interactive

This command starts the docker container in interactive mode. You will find yourself in a command prompt and have access to all the

tools installed in the docker container.

Normally this should not be necessary for the course, but can be used for troubleshooting.

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General Makefile Targets

\$ make gtkwave

This command starts GTKWave using the docker container without a waveform loaded.

With it you can view the simulation results for your cipher.



General Makefile Targets

\$ make klayout

This command starts KLayout using the docker container without a design loaded.

Klayout is a capable layout viewer and will be used to visualize the layout of your cipher and the final chip.



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Makefile Targets - Exercise 1 \$ make ex1-lint

Runs verilator in linting mode over your design to detect issues that can lead to problems.

Make sure to fix all warnings. Otherwise this might lead to problems later on.

\$ make ex1-openlane

Starts the physical process of hardening cipher_core using the sky130A PDK.

Actually, OpenLane 2 is used to harden your ciper. OpenLane 2 is the successor to OpenLane.

Flansed: 0.000s Nemory: 943.00M "merged" in: sky130A mr.drc:439 Polygons (raw): 938 (flat) 938 (hierarchical) Elapsed: 0.080s Memory: 943.00M outside part" in: sky130A mr.drc:439 Edges: 0 (flat) 0 (hierarchical) Elapsed: 0.010s Memory: 943.00M space" in: sky130A mr.drc:441 Edge pairs: 0 (flat) 0 (hierarchical) Flansed: 0.040s Nemory: 959.00M "output" in: sky130A mr.drc:441 Edge pairs: 0 (flat) 0 (hierarchical) Elapsed: 0.000s Memory: 943.00M "separation" in: sky130A mr.drc:443 Edge pairs: 0 (flat) 0 (hierarchical) Elapsed: 0.020s Memory: 959.00M "space" in: sky130A mr.drc:443 Edge pairs: 0 (flat) 0 (hierarchical) Elapsed: 0.020s Memory: 943.00M ** in: sky130A mr.drc:443 Edge pairs: 0 (flat) 0 (hierarchical) Elapsed: 0.080s Memory: 943.00M "output" in: sky1304 mr. drc:443 Edge pairs: 0 (flat) 0 (hierarchical) Elapsed: 0.010s Memory: 943.00M "input" in: sky130A mr.drc:447 Polygons (raw): 50570 (flat) 2546 (hierarchical) Flapsed: 0.010s Nemory: 943.00M "enclosing" in: sky130A mr.drc:449 Classic - Stage 56 - Design Rule Check (KLayout)

\$ make ex1-openroad

Loads the latest stage from "ex1-openlane" into OpenROAD to visualize the design. This can be useful if the hardening process fails due to routing conqestion etc.

To save an image of your design execute "save_image image.png" in the tcl command line.



\$ make ex1-klayout

Opens the layout of your design from ex1/results in Klayout.

To save a high-resolution image, open: Macros \rightarrow Macro Development

Then execute in the console:

RBA::Application.instance.main_window

.current_view.save_image("image.png",2000,2000)



\$ make ex1-cocotb

Runs RTL simulation of your design using cocotb as the testbench environment.

You can write your testbench in Python under ex1/tb/.

For RTL simulation, Verilator is used as the simulator.

0.0015 INFD	cocoth	Running on Verilator version 5.018 2023-10-30
Q.QBas IAFD	cocath	Barning tests with cocate x1.8.1 from /usr/lacel/lib/pythan1.18/dist-packages/cac
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		11 th carath sizele test 0455 11645.00 8 16 62687.47

\$ make ex1-cocotb-gl

Runs GL simulation of your design using cocotb as the testbench environment.

The same testbench under ex1/tb/ is used with \$GL set to 1.

For GL simulation, Icarus Verilog is used as the simulator.

```
Running on Icarus Verilog version 13.0 (devel)
                                                                    Remning tests with cocotb vi.0.1 from /urr/local/lib/pythan3.10/dist-packages/cocotb
Seeding Python random module with 1707096014
Ite.py17b: UserNarning: Python runners and associated APIs are an experimental feature and
0.00ms EMPO cocotb
/usr/LLb/python3/dist-packages
exec(co, module.__dict__)
                                                                       Front test th coroth simple test
    0.0015 LAFO
                                                                        running simple_test [1/1]
TODO Simple test for cipher core
ST info: damafile dama.fat esered for extent
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                                                                       finish_o:
Test_finished!
                                                                      ** TEST STATUS SID TIME (ns) REAL TIME (s) RATED (ns/s) **
                                                                      ** tb_cocotb.simple_test PMSS 12045.00 0.32 37022.16 **
                                                                      ** TESTS=1 PASS=1 FAIL=0 SKIP=0 12045.09 0.07 10038.63 **
```

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Makefile Targets - Exercise 1

\$ make ex1-gtkwave

After running RTL or GL simulation for exercise 1 the resulting waveform "dump.fst" is saved under ex1/tb/sim_build.

This make target starts GTKWave with "dump.fst" loaded.

		GTKWave - ex1/tb/sim_build/dump.t	fst		
File Edit Search Time Ma	arkers View Help				
* • • • • •	SKX X > From: 0 sec	To: 12045001 ps	C	Marker	3 286 000 ps
▼ SST	Tine	1 45 2 45	3.05		6
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wire indata_ready_o	indata valid i=1				
wire indata valid i	key_1[127:0]=00	0304(0003030)			
wire key i[127:0]	nonce_1[127:0]=00	000000000000000000000000000000000000000			
wire paper (127-0)	outdata_0[127:0]=00	00000000000			
mice conducts of 127-01	outdata_ready_1=1				
whe outdata_o(127:0)	outdata_valid_o=0				
whe outdata_ready_i	rst_n1=1				
wire outdata_valid_o	start_1=1				
Q	rad_o[151;0]+00				
Append Insert B	eplace				

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Makefile Targets - Exercise 2 \$ make ex2-lint

Runs verilator in linting mode over your design to detect issues that can lead to problems.

Make sure to fix all warnings. Otherwise this might lead to problems later on.

<pre>%Error: ex2/src/cipher_peripheral.sv:2</pre>	3:29: Can't find definition of variable: 'test123'
23 assign bus_master.req = te	st123;
^~	ne he he he
<pre>%Error: ex2/src/cipher_peripheral.sv:2</pre>	4:30: Can't find definition of variable: 'test234'
	: Suggested alternative: 'test123'
24 assign bus_master.addr = t	est234;
	he he he he
%Error: ex2/src/cipher_peripheral.sv:2	5:28: Can't find definition of variable: 'test345'
	: Suggested alternative: 'test234'
25 assign bus_master.we = tes	t345;
^~~~	No No No No
%Error: Exiting due to 3 error(s)	
make: *** [Makefile:129: ex2-lint] Feh	ler 1

\$ make ex2-openlane

Starts the physical process of hardening cipher_core using the sky130A PDK.

Actually, OpenLane 2 is used to harden your ciper. OpenLane 2 is the successor to OpenLane.

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Circuit sky130_fd_sc_Mfill_2 contains no Contents of circuit 1: Circuit: "cipter unc Circuit cipter uncaper est contains 97560 de Cinas: sky120_fd_sc_Mbd_2_initianes: 10 Cinas: sky120_fd_sc_Mbd_2_initianes: Cinas: sky120_fd_sc_Mcoreb_11 initianes: Cinas: sky120_fd_sc_Mcoreb_11 initianes: Cinas: sky120_fd_sc_Mcoreb_11 initianes:	devices. DDDer so2' evice instances.
Contents of circuit 1: Circuit: 'Cipter wro Circuit cipter wrogaer e2 contains \$7366 de Class: sky126 fd.sc.Md_bof_2 instances: 10 Class: sky126 fd.sc.Md_bof_2 instances: 10 Class: sky126 fd.sc.Md_corb_1 instances: 10 Class: sky126 fd.sc.Md_corb_1 instances: 10 Class: sky126 fd.sc.Md_corb_1 instances: 10	autor es2' evice instances.

\$ make ex2-openroad

Loads the latest stage from "ex2-openlane" into OpenROAD to visualize the design. This can be useful if the hardening process fails due to routing conqestion etc.

To save an image of your design execute "save_image image.png" in the tcl command line.



Makefile Targets - Exercise 2 \$ make ex2-klayout

Opens the layout of your design from ex2/results in Klayout.

To save a high-resolution image, open: Macros \rightarrow Macro Development

Then execute in the console: RBA::Application.instance.main_window .current_view.save_image("image.png",2000,2000)



\$ make ex2-cocotb

Runs RTL simulation of your design using cocotb as the testbench environment.

You have to write your own program under /ex2/sw/. Set \$PROGRAM to the active program e.g. hello-world.

For RTL simulation, Verilator is used as the simulator.

INFO: Running comman	d /foss/designs/ex2/tb/sim_build/tb	_top in directory /foss/designs/ex2/tb/sim_build
al anvironment lisin	a system-wide Buthon interpreter	Lines Mr_ensetebbles
THE THE	ani	(ani/Gnifement cro:10) in ani print registered impl. VPI registered
0 for THEO	991	The second secon
0.00ms Inro	COLOTO	Roming on verifator version 3.010 2023 10-30
0.00ms Inro	COLOTO	Roming Cests with Cocord VI.a.1 Free Justice (CLD/ pythons. Invalst-packages/cocord
0.00hs Inro	COLOTO	seeding rython random monite with 1707099734
ages (res by tunnas are	c.bacwades/_bicescieseicrouviewitt	e.py:1/o: userwarning: python runners and associates wris are an experimental reature a
subject to change.		
exec(co, module	dict)	
0.00ns IMFO	cocotb.regression	Found test tb_cocotb.simple_test
0.00ns IMFO	cocotb.regression	running simple_test (1/1)
		This test runs the program under sw/
Loading ROM content	from//sw/program0.vmem	
coading ROM content	from//sw/program1.vmem	
50.00ns IMFO	cocotb.tb_top	Reset done
Simulation output:		
Hello World!		
10040 00os TNFO	coroth rearession	simple test passed
10040 00os INFO	coroth rearession	
LOCIOLICOUL LUI O		** TEST STATUS SIN TIME (os) BEAL TIME (s) BATTO (ps/s) **
		11 th cocoth cipple test DALS 310540.00 1.45 167415.34 18
		10 101010.510pte_test PASP 310940.00 1.45 107415.34
		14 TETE-3 DATE-1 FATL-0 SETE-0 310040 00 3 31 340300 00 48
		Itolas respected and an and a star

\$ make ex2-cocotb-gl

Runs GL simulation of your design using cocotb as the testbench environment.

Same as ex2-cocotb, but \$GL is set to 1 and the gate level files for cipher_peripheral are used. For GL simulation, Icarus Verilog is used as the simulator.

VFG: Running comme	nd wvp -M /usr/local/lib/python3	.10/dist-packages/cocoth/libs -m libcocotbypi_icarus /foss/designs/ex2/th/sim_build/sim.vv
st in directory /1	oss/designs/ex2/tb/sim_duitd	shed/ani eshed ros:75 in rat scorras name is yony
and rement. list	an system-wide Puthan interprete	The state of the s
LUCION IMPO	opi	. /api/GpiGommon.com/101 in moi arint registered impl VPI registered
0 0fox TMF0	cacath	Busine of Trans Mariles version 11.8 (deset)
8.88os IMED	cecath	Bunning tests with roroth x1.8.1 from /usr/local/lib/ovthon3.18/dist.packages/coroth
0 Office TMED	cacath	Sentian Dathan candas module with 1267503681
sr/lib/mthro3/41	st.sarkases/ rutest/assertios/re	write res128: liserBarning: Puthan numers and associated 491s are an experimental feature
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erecice, manule	dict)	
0 Olor TMCO	cecath regression	Erend text th counth simple text
0 0for TMF0	cacalb repression	funding should fast (1/1)
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radios ROM contest	free ((sw/prepren) yees	
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58 BROS THEB	cacalh Ib Ion	Beset three
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ello World!		
erce sorear		
10140 Blos TMED	cacath repression	simple test associ
10140.00ns IMPO	cacath, repression	
		** TEST STATUS STN TIME (os) REALTINE (s) RATIO (os(s))
		11 th caroth size and the test 0455 310548 06 6.62 46951 28 -
		** TESTS=1 PASS=1 FAIL=0 SKIP=0 310040.00 6.55 44582.26

Makefile Targets - Exercise 2 \$ make ex2-gtkwave

After running RTL or GL simulation for exercise 2 the resulting waveform "dump.fst" is saved under ex2/tb/sim_build.

This make target starts GTKWave with "dump.fst" loaded.



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\$ make tapeout-chip_art

- Starts a Klayout Python script to convert the PNG image under tapeout/chip_art/chip_art.png to .gds. A tcl script for Magic creates a .lef file.
- Feel free to change the image, but make sure to keep the resolution.

Creating macro of size 1000 µm x 500 µm Magic 8.3 revision 452 - Compiled on Mon Feb 12 03:05:47 PM CET 2024. Starting magic under Tcl interpreter Using the terminal as the console. Using NULL graphics device. Processing system .magicrc file Sourcing design .magicrc for technology sky130A ... 2 Magic internal units = 1 Lambda Input style sky130(): scaleFactor=2. multiplier=2 The following types are not handled by extraction and will be treated as non-electrical types: ubm Scaled tech values by 2 / 1 to match internal grid scaling Loading sky130A Device Generator Menu Loading "gds2lef.tcl" from command line. Input style sky130(vendor): scaleFactor=2, multiplier=2 CIF input style is now "sky130(vendor)" Warning: Calma reading is not undoable! I hope that's OK. Library written using GDS-II Release 6.0 Library name: LIB Reading "chip art". Generating LEF output chip art.lef for cell chip art: Diagnostic: Write LEF header for cell chip art Diagnostic: Writing LEF output for cell chip art Diagnostic: Scale value is 0.005000

\$ make tapeout-rom

- Starts OpenRAM (or you could say OpenROM) to create a ROM macro for your program.
- Set \$PROGRAM to the active program e.g. hello-world.

	OpenRAM V1.2.48		
	VLSI Design and Automation Lab		
	Computer Science and Engineering Department		
	University of California Santa Cruz		
	Usage help: openram-user-group@ucsc.edu		
	Development help: openram-dev-group@ucsc.edu		
	See LICENSE for license info		
* Start: 02/1	4/2024 09:41:52		
Output files a	re:		
foss/designs/	tapeout/rom/macro/sky130 rom 4kbyte 32 inst0/sky130 r	om 4kbyte 32 i	nst0.sp
foss/designs/	tapeout/rom/macro/sky130 rom 4kbyte 32 inst0/sky130 r	om 4kbyte 32 i	nst0.v
foss/designs/	tapeout/rom/macro/sky130 rom 4kbyte 32 inst0/sky130 r	om 4kbyte 32 i	nst0.lef
foss/designs/	tapeout/rom/macro/sky130 rom 4kbyte 32 inst0/sky130 r	om 4kbyte 32 i	nst0.ads
reate rom of	word size 4 with 1024 num of words		

\$ make tapeout-final

The final step to complete tapeout!

This target calls a Klayout Python script to merge the layouts of your cipher, the ROMs and the chip_art with the pre-hardened chip.

Congratulations, your design is finished!

Replacing instance CH cipher_wrapper_ex2 with GDS ex2/results/dds, Replacing instance CH_sky130_rom 4kbyte_32_inst0 with GDS tapeout/ yte_32_inst0/sky130 rom 4kbyte_32_inst0.gds Replacing instance CH_sky130_rom 4kbyte_32_inst1 with GDS tapeout/ yte_32_inst1/sky130 rom 4kbyte_32_inst1.gds Replacing instance CH_chip_art with GDS tapeout/chip_art/chip_art

\$ make tapeout-klayout

Opens the layout of your design

chip_tapeout.gds in Klayout.

To save a high-resolution image, open: Macros \rightarrow Macro Development

Then execute in the console: RBA::Application.instance.main_window .current_view.save_image("image.png",2000,2000)



Verilator is a free and open-source software tool which converts Verilog to a cycle-accurate behavioral model in C++ or SystemC. Verilator is the fastest Verilog/SystemVerilog simulator.

Website: https:

//www.veripool.org/verilator/



Icarus Verilog is an implementation of the Verilog hardware description language compiler that generates netlists in the desired format. It supports the 1995, 2001 and 2005 versions of the standard, portions of SystemVerilog, and some extensions.

Repository: https:

//github.com/steveicarus/iverilog



cocotb is an open source coroutine-based cosimulation testbench environment for verifying VHDL and SystemVerilog RTL using Python.

Website: https://www.cocotb.org/



GTKWave is an open source waveform viewer and can read various formats such as fst and vcd files.

Repository: https: //github.com/gtkwave/gtkwave



Open Source Tools OpenROAD

OpenROAD's unified application implementing an RTL-to-GDS Flow.

Repository: https://github.com/ The-OpenROAD-Project/OpenROAD Documentation: https://openroad. readthedocs.io/en/latest/



Open Source Tools OpenLane 2

The next generation of OpenLane, rewritten from scratch with a modular architecture

Repository: https: //github.com/efabless/openlane2 Documentation: https://openlane2.readthedocs.io/ en/latest/



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Open Source Tools Magic VLSI Layout Tool

Magic is a venerable VLSI layout tool, written in the 1980's at Berkeley by John Ousterhout. With well thought-out core algorithms, Magic is a powerful yet simple tool for circuit layout and validation.

Repository: https://github.com/ RTimothyEdwards/magic



KLayout chip mask layout viewing, editing and more. It provides an extensive Ruby and Python API. Website: https://www.klayout.de/

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Open Source Tools OpenRAM

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An open-source static random
access memory (SRAM) compiler.
Website: https://openram.org/
Repository:
https://github.com/VLSIDA/OpenRAM
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Open Source Tools Further Links I

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