Side-Channel Security

Chapter 6: Software-based Fault Attacks

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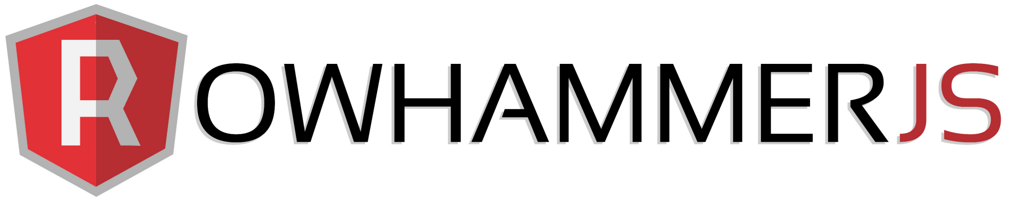
www.iaik.tugraz.at

ROWHAMMER

CTV



ROOT privileges for web apps!

Test - Mozilla Firefox (on lab02)

Test

file:///home/dgruss/rowhammerjs/rowhammer.html

Search

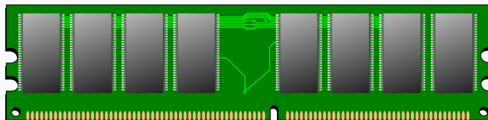
320: 12
330: 9
340: 1
350: 0
360: 1
370: 2
380: 199
390: 76
400: 72
410: 231
420: 572
1250
[!] Found flip (254 != 255) at array index 340021386 when hammering indices 339881984 and 340156416

[!] Found flip (239 != 255) at array index 340022176 when hammering indices 339881984 and 340156416

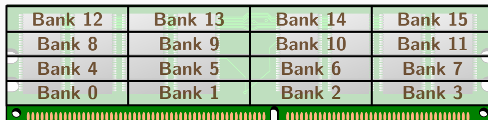
[!] Found flip (191 != 255) at array index 340023138 when hammering indices 339881984 and 340156416

[!] Found flip (254 != 255) at array index 340025146 when hammering indices 339881984 and 340156416

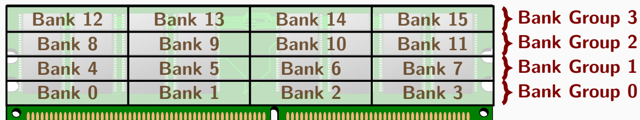
DRAM organization

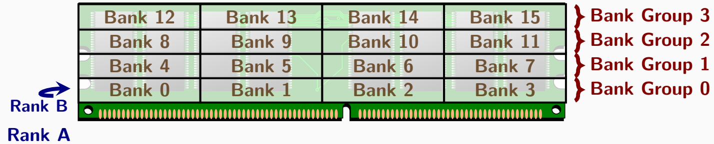


DRAM organization

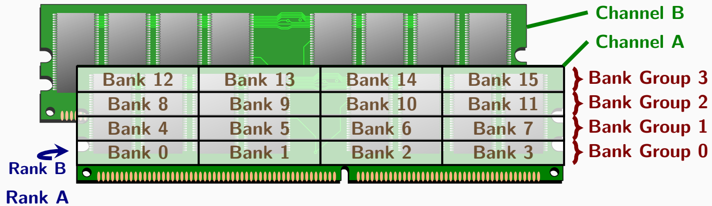


DRAM organization

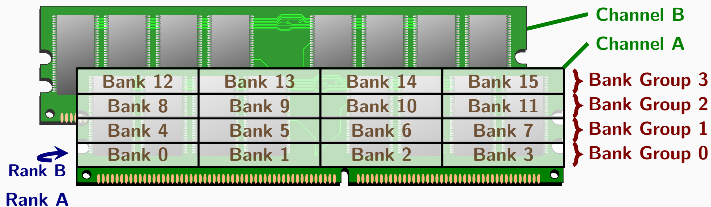



Bank 12
Bank 13
Bank 14
Bank 15
Bank 8
Bank 9
Bank 10
Bank 11
Bank 4
Bank 5
Bank 6
Bank 7
Bank 0
Bank 1
Bank 2
Bank 3
Bank Group 3
Bank Group 2
Bank Group 1
Bank Group 0
Rank B
Rank A

DRAM organization

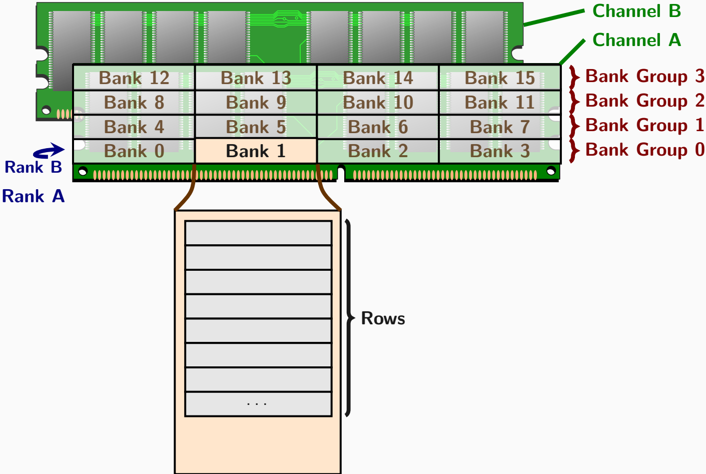


DRAM organization

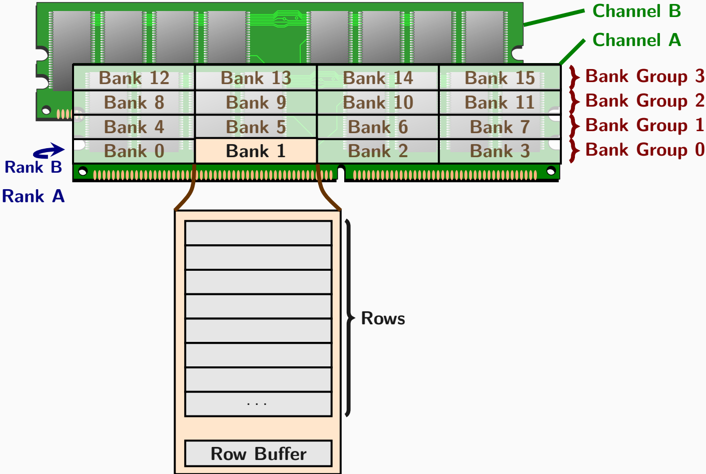


4 banks $\times$ 4 bank groups $\times$ 2 ranks $\times$ 2 channels $=$ 64 banks total

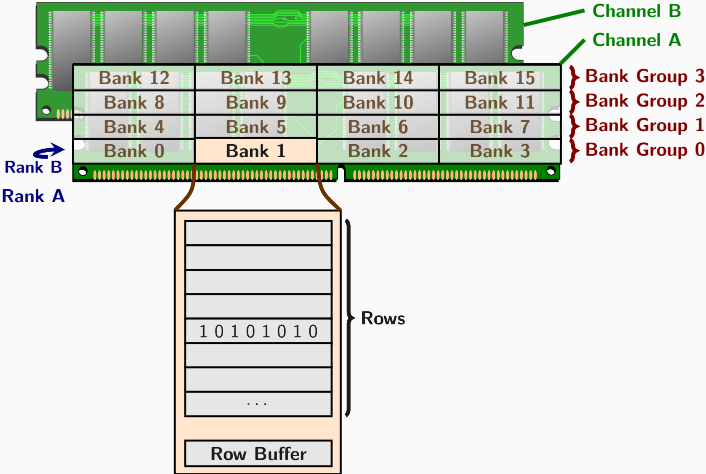
DRAM organization

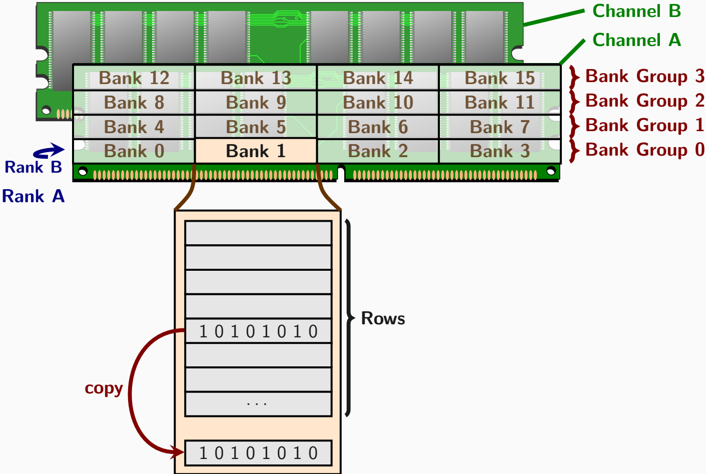


DRAM organization

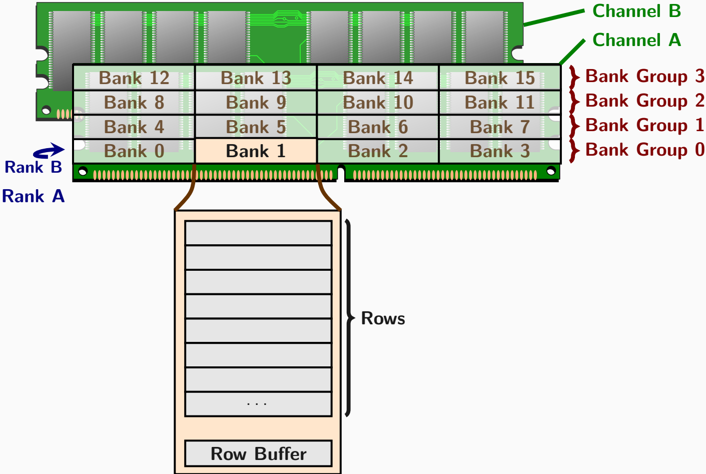


DRAM organization

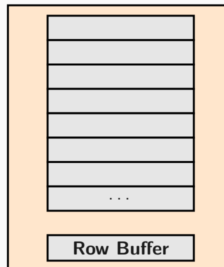



Channel B
Channel A
Bank 12
Bank 13
Bank 14
Bank 15
Bank 8
Bank 9
Bank 10
Bank 11
Bank 4
Bank 5
Bank 6
Bank 7
Bank 0
Bank 1
Bank 2
Bank 3
Bank Group 3
Bank Group 2
Bank Group 1
Bank Group 0
Rank B
Rank A
1 0 1 0 1 0 1 0
...
Rows
copy
1 0 1 0 1 0 1 0

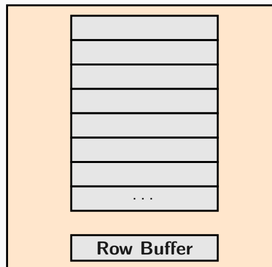
DRAM organization



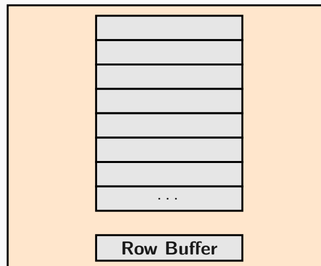
DRAM organization

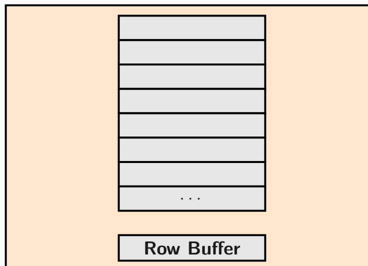


DRAM organization

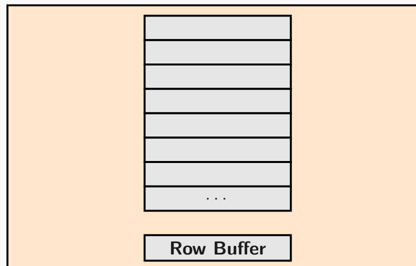


DRAM organization

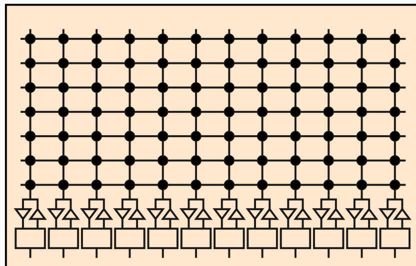



...
Row Buffer

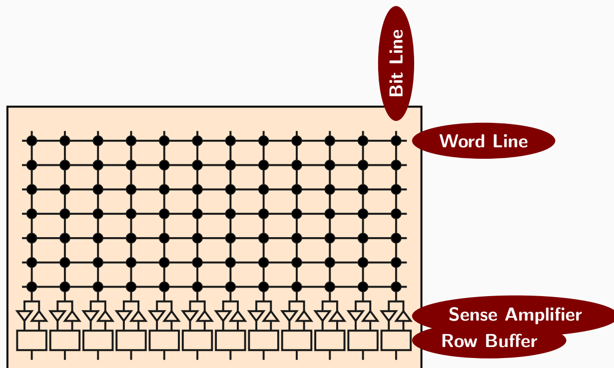
DRAM organization



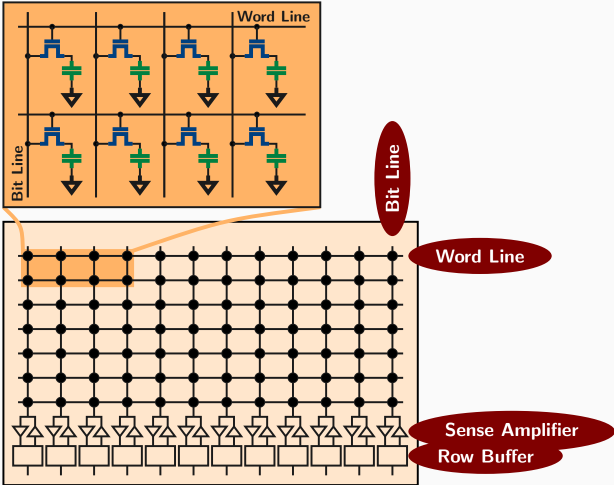
DRAM organization

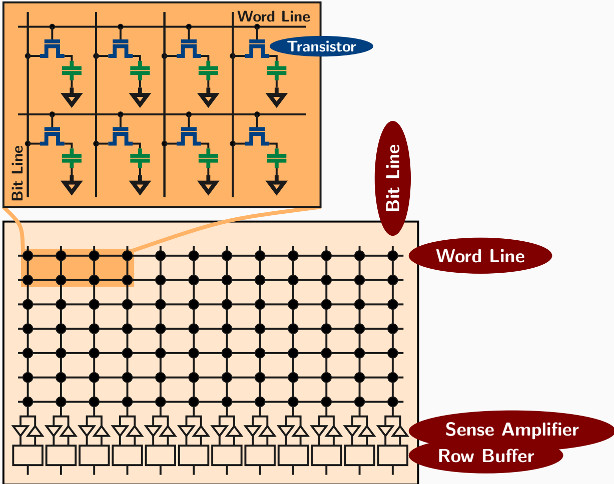


DRAM organization

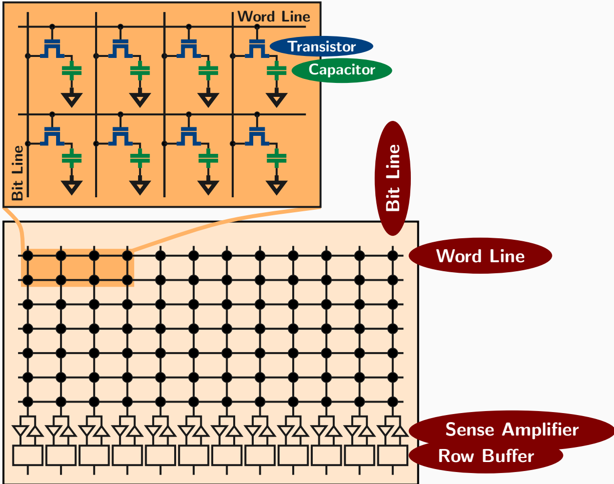


DRAM organization

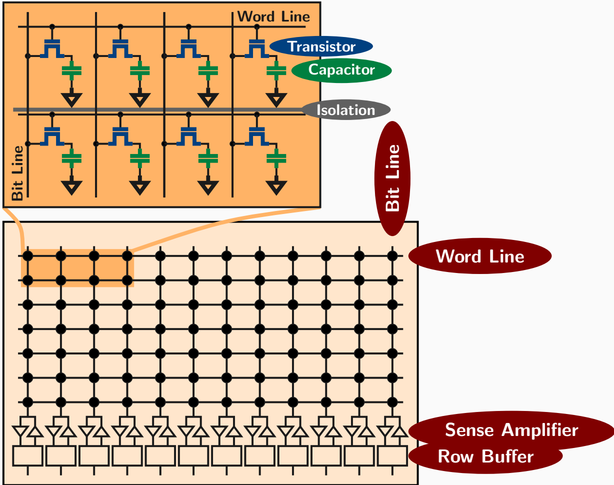



Word Line
Transistor
Bit Line
Bit Line
Word Line
Sense Amplifier
Row Buffer

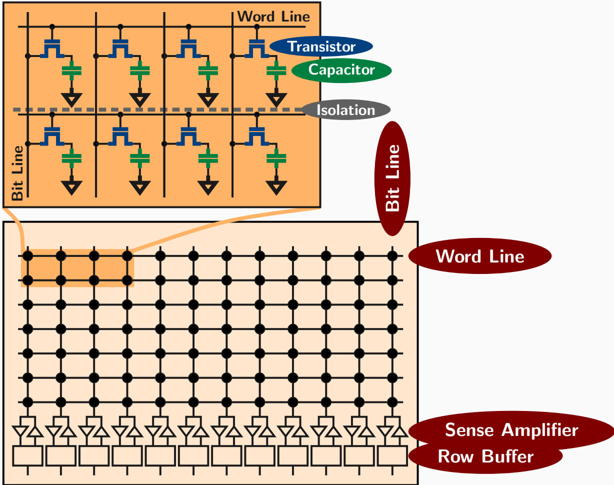
DRAM organization



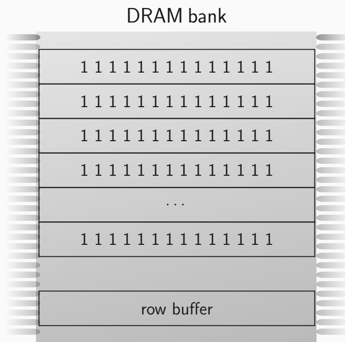
DRAM organization



DRAM organization

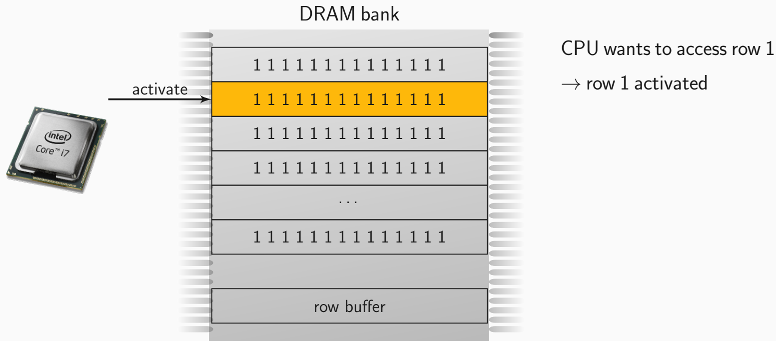


How reading from DRAM works



CPU wants to access row 1

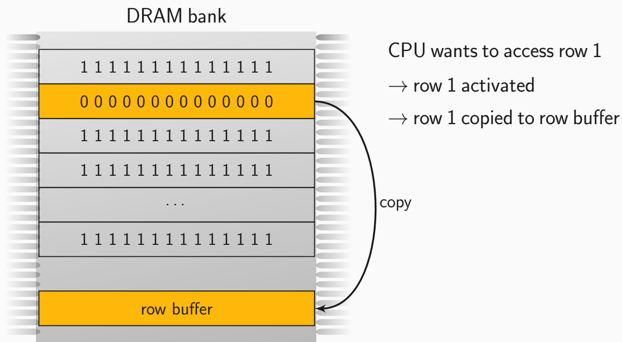
How reading from DRAM works



CPU wants to access row 1

→ row 1 activated

How reading from DRAM works

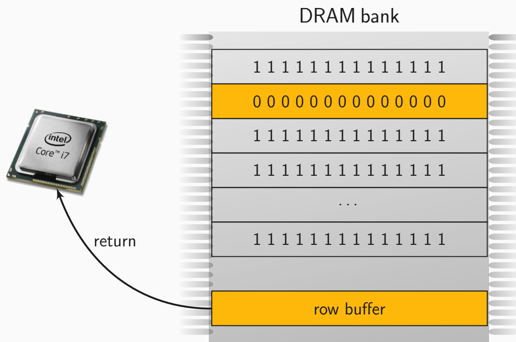


CPU wants to access row 1

→ row 1 activated

→ row 1 copied to row buffer

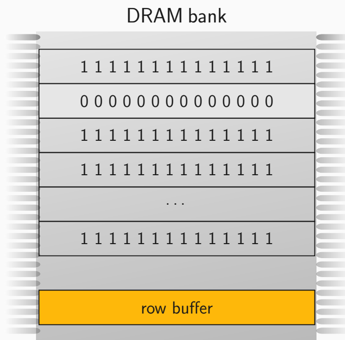
How reading from DRAM works



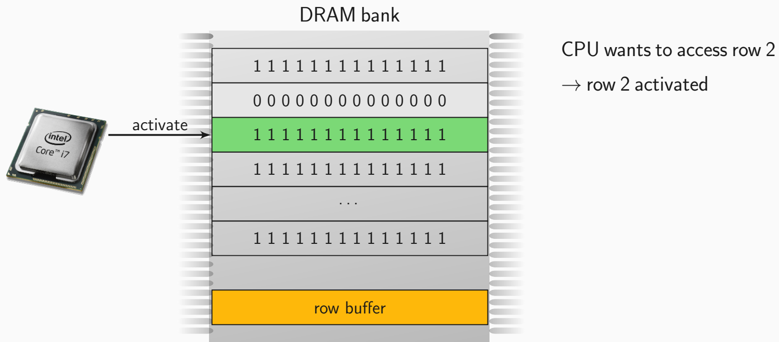
CPU wants to access row 1

→ row 1 activated

→ row 1 copied to row buffer



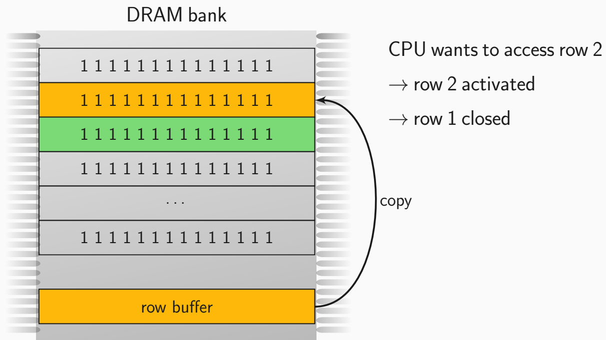
CPU wants to access row 2



CPU wants to access row 2

→ row 2 activated

How reading from DRAM works

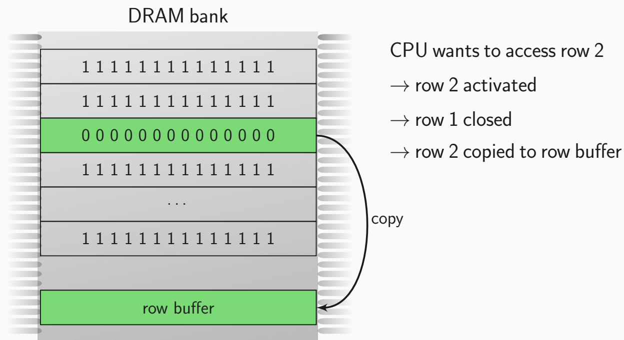


CPU wants to access row 2

→ row 2 activated

→ row 1 closed

How reading from DRAM works



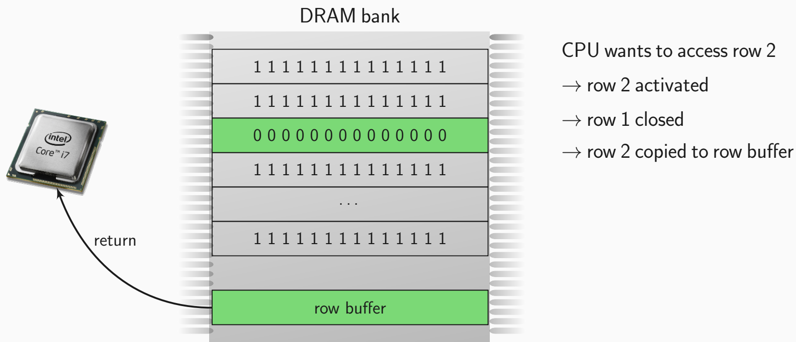
CPU wants to access row 2

→ row 2 activated

→ row 1 closed

→ row 2 copied to row buffer

How reading from DRAM works



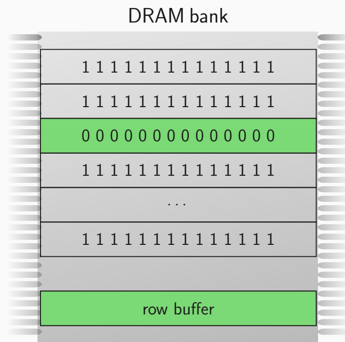
CPU wants to access row 2

→ row 2 activated

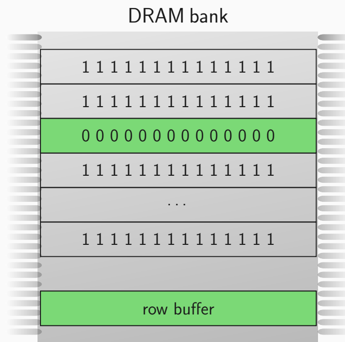
→ row 1 closed

→ row 2 copied to row buffer

How reading from DRAM works

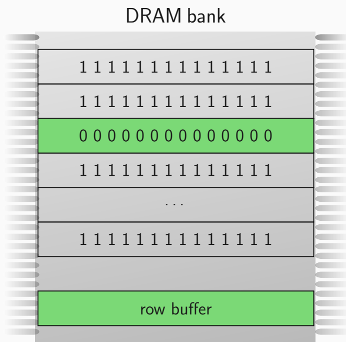


→ slow (row conflict)



CPU wants to access row 2—again

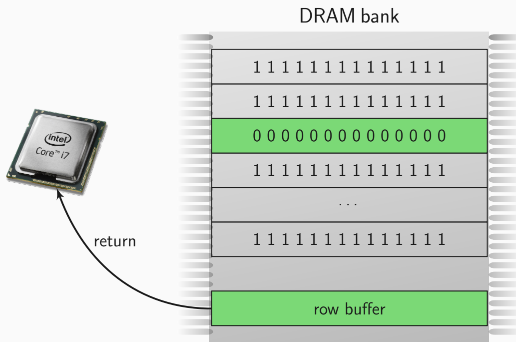
How reading from DRAM works



CPU wants to access row 2—again

→ row 2 already in row buffer

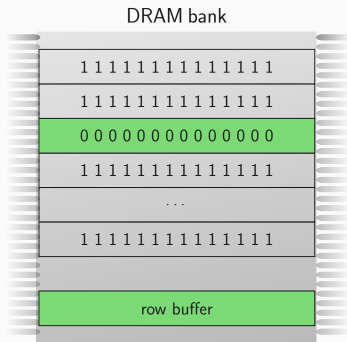
How reading from DRAM works



CPU wants to access row 2—again

→ row 2 already in row buffer

How reading from DRAM works

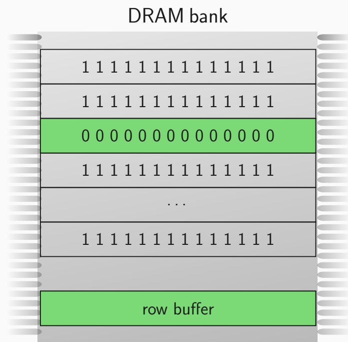


CPU wants to access row 2—again

→ row 2 already in row buffer

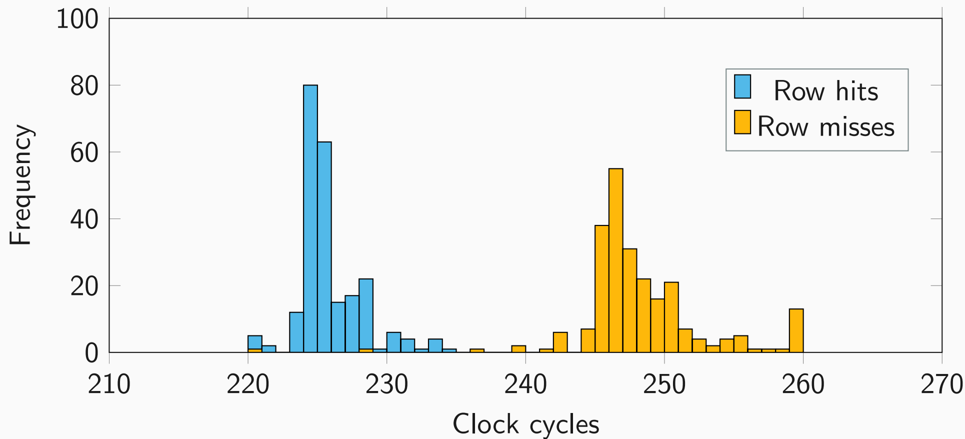
→ fast (row hit)

How reading from DRAM works

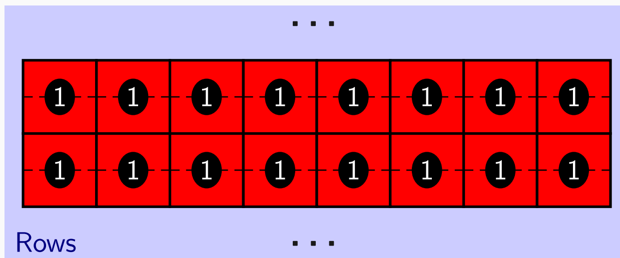


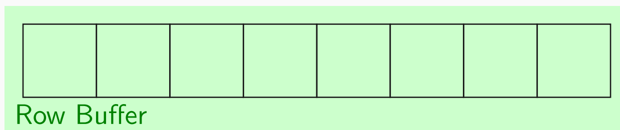
row buffer = cache

Timing difference

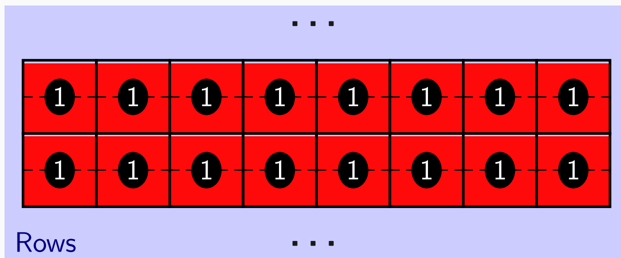


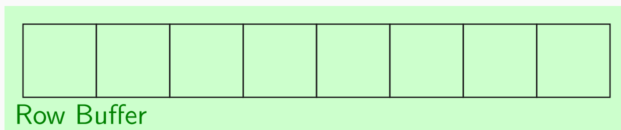
Cell Discharge

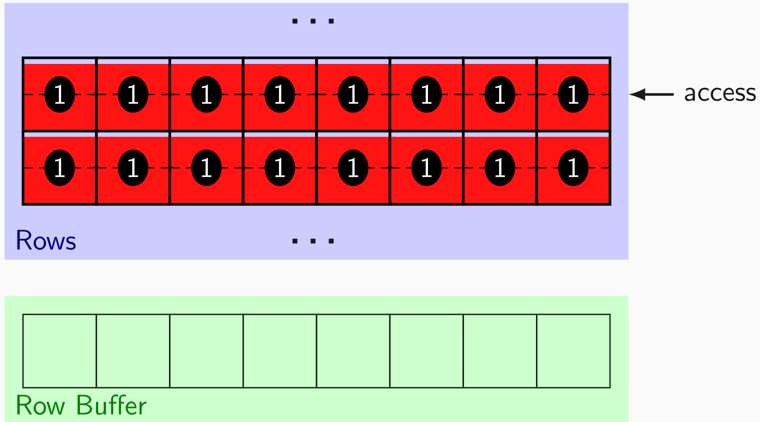




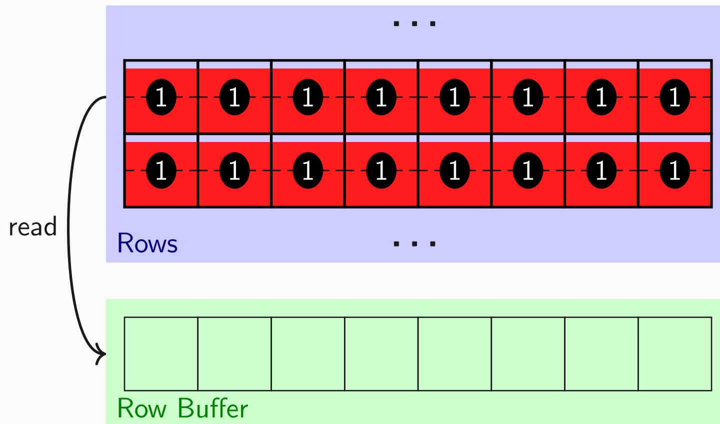
Cell Discharge

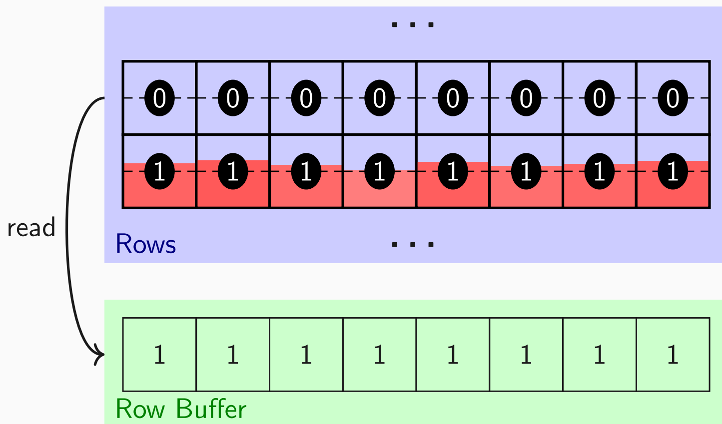




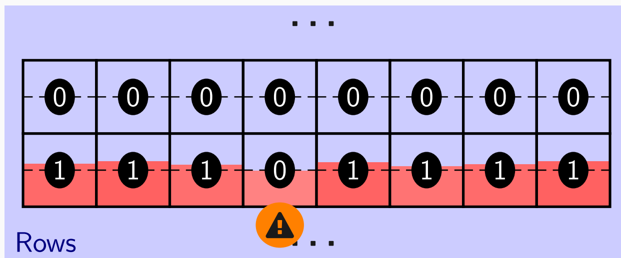

...
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
access
Rows
...
Row Buffer

Cell Discharge

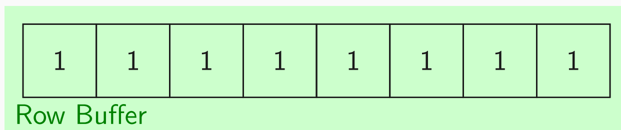




...
0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1
read
Rows
...
1 1 1 1 1 1 1 1
Row Buffer

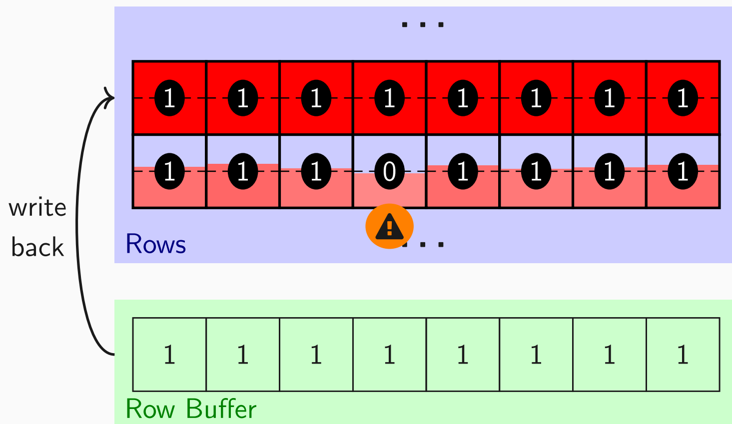


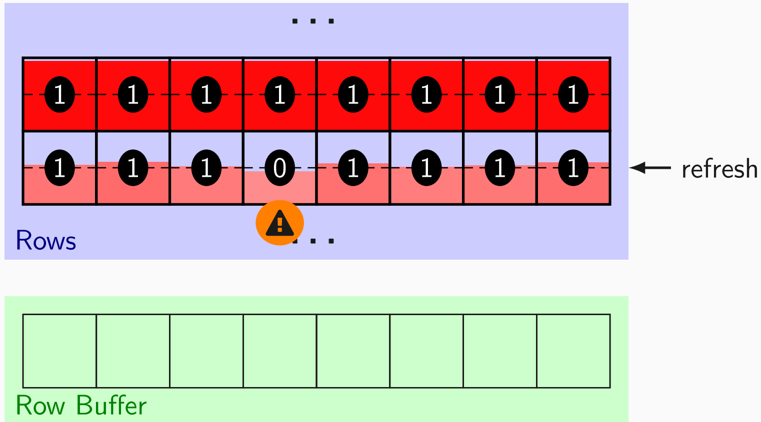
...
0 0 0 0 0 0 0 0
1 1 1 0 1 1 1 1
Rows
...



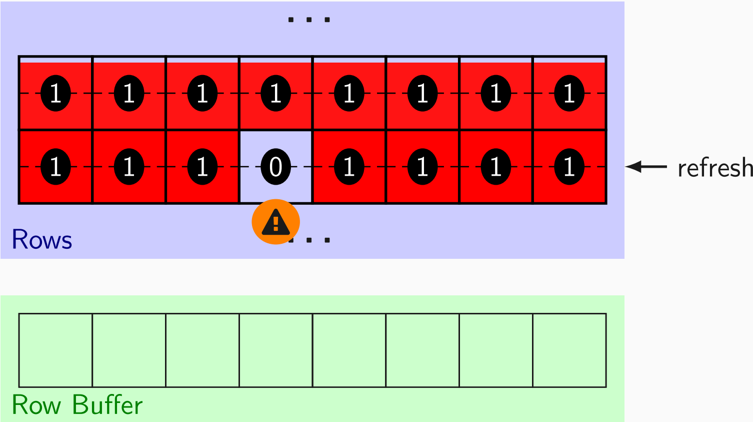
1 1 1 1 1 1 1 1
Row Buffer

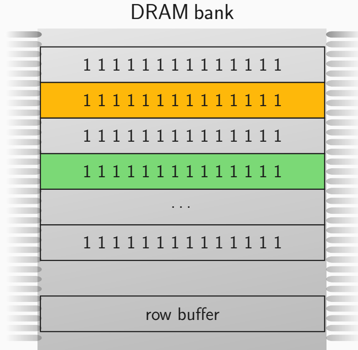
Cell Discharge

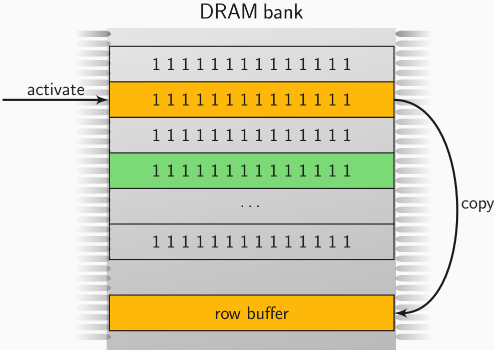


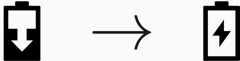

...
1 1 1 1 1 1 1 1
1 1 1 0 1 1 1 1
refresh
Rows
...
Row Buffer

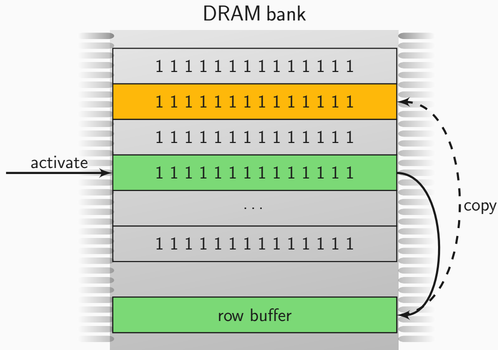
Cell Discharge

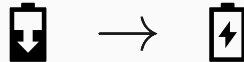



DRAM bank
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
...
1 1 1 1 1 1 1 1 1 1 1 1 1 1
row buffer

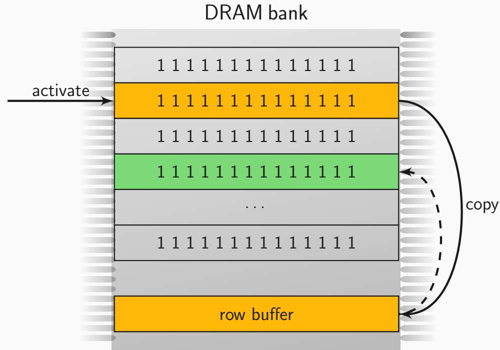

DRAM bank
activate
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
. . .
1 1 1 1 1 1 1 1 1 1 1 1 1 1
row buffer
copy

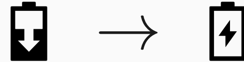




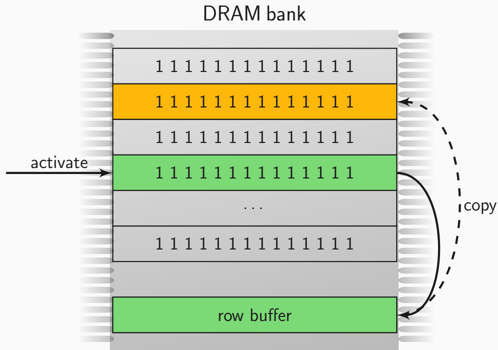


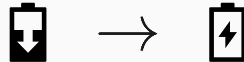
Cells leak faster upon proximate accesses → Rowhammer



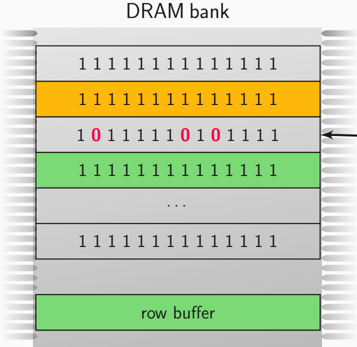


Cells leak faster upon proximate accesses → Rowhammer

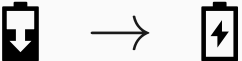




Cells leak faster upon proximate accesses → Rowhammer



bit flips in row 2!



Cells leak faster upon proximate accesses → Rowhammer

How widespread is the issue?

How widespread is the issue?

How widespread is the issue?

- 85% affected [20] (see Figure)

How widespread is the issue?

- 85% affected [20] (see Figure)

- First believed to be safe

How widespread is the issue?

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- 85% affected [20] (see Figure)

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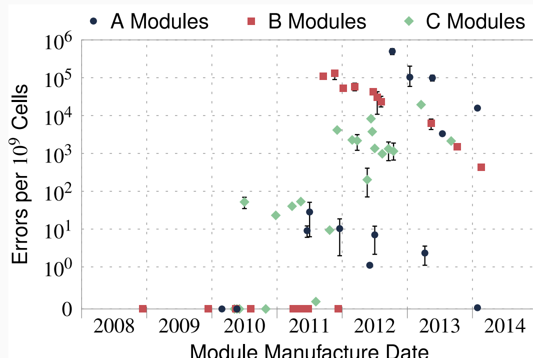
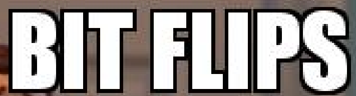



BIT FLIPS
BIT FLIPS EVERYWHERE

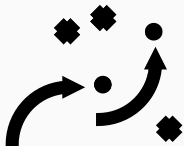
Requirements

Memory accesses must be

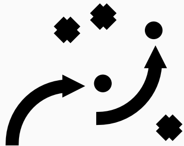
- uncached: reach DRAM
- fast: race against the next row refresh
- targeted: reach specific row

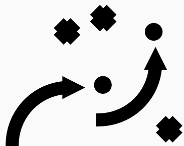
How do we get enough uncached accesses?

Access techniques

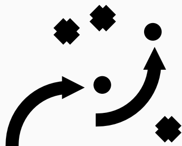


Access techniques





- `clflush` instruction → original paper [20]



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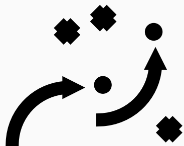

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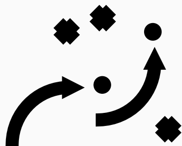
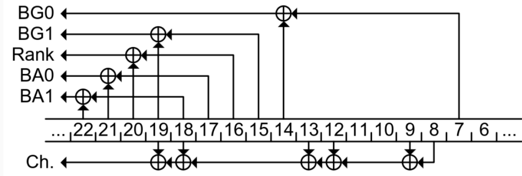
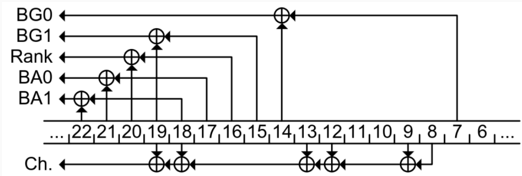


- `clflush` instruction → original paper [20]
- cache eviction [2, 13]
- non-temporal accesses [27]
- uncached memory [33]

How do we target accesses?



- fixed map: physical addresses → DRAM cells



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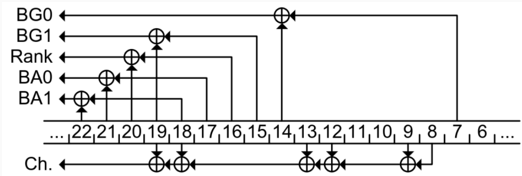

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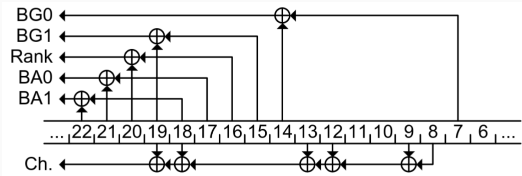

- fixed map: physical addresses → DRAM cells
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- using the timing difference between row hits and row conflicts

How to exploit random bit flips?

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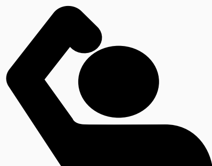

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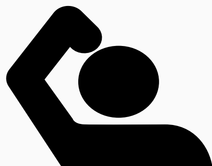

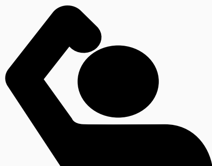

- They are not random → highly reproducible flip pattern!

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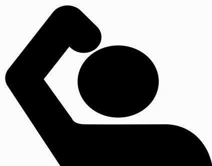

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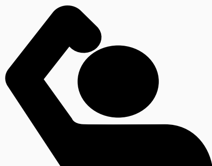

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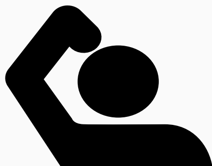

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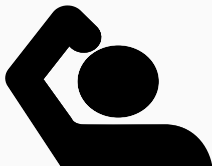

- They are not random $\rightarrow$ highly reproducible flip pattern!
  1. Choose a data structure that you can place at arbitrary memory locations
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  3. Place data structure there
  4. Trigger bit flip again

Page Table Entries

P	RW	US	WT	UC	R	D	S	G		
										X

Page Table Entries

P	RW	US	WT	UC	R	D	S	G	Ignored	
				Ignored						X

Page Table Entries

P	RW	US	WT	UC	R	D	S	G	Ignored	

Physical Page Number

	Ignored	X

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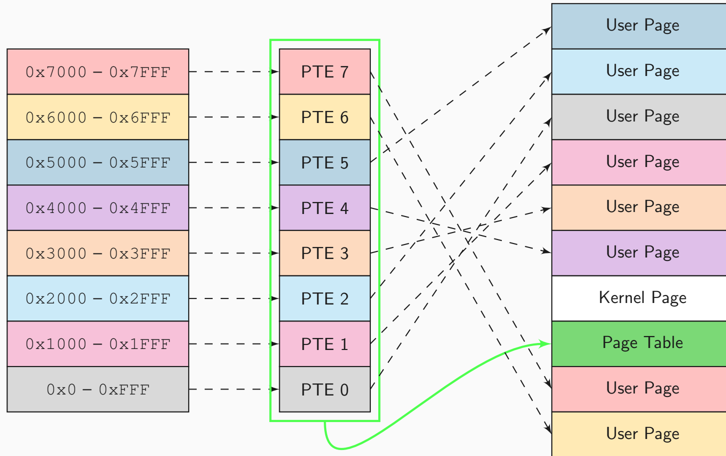
Physical Page Number

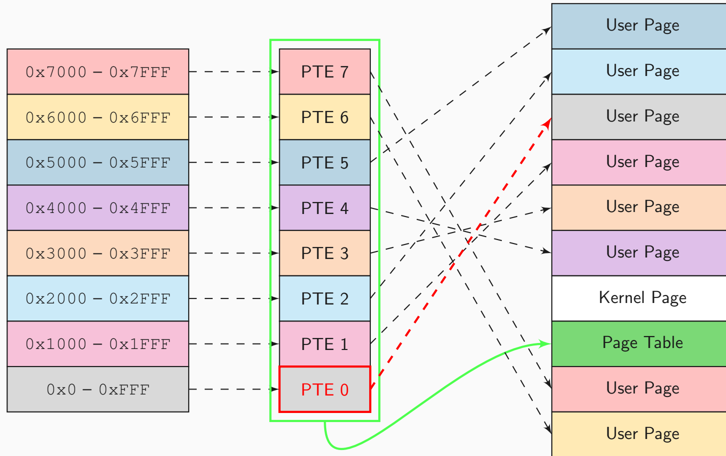
	Ignored	X

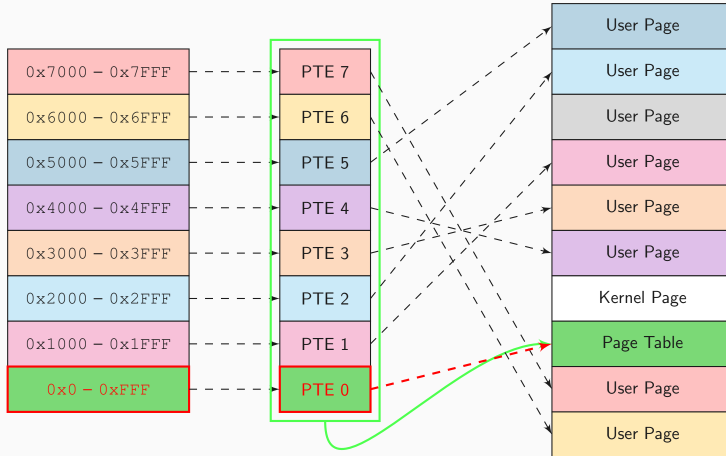
Each 4 KB page table consists of 512 such entries

Page Table Manipulation



Page Table Manipulation

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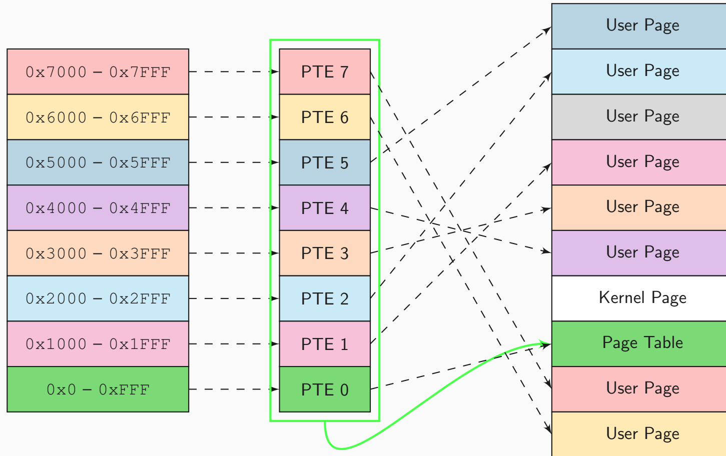
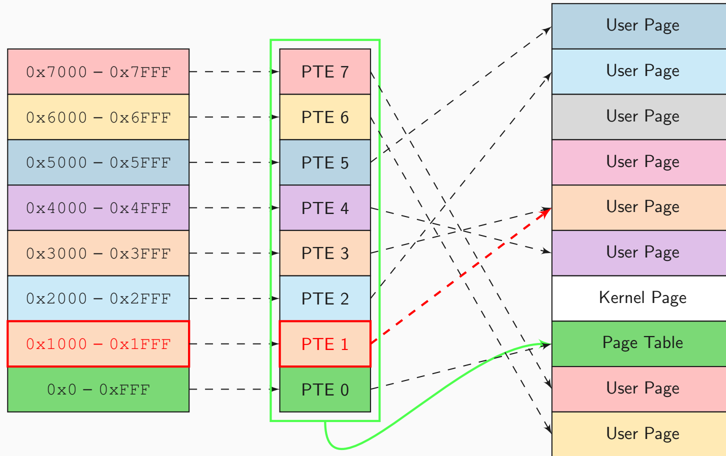
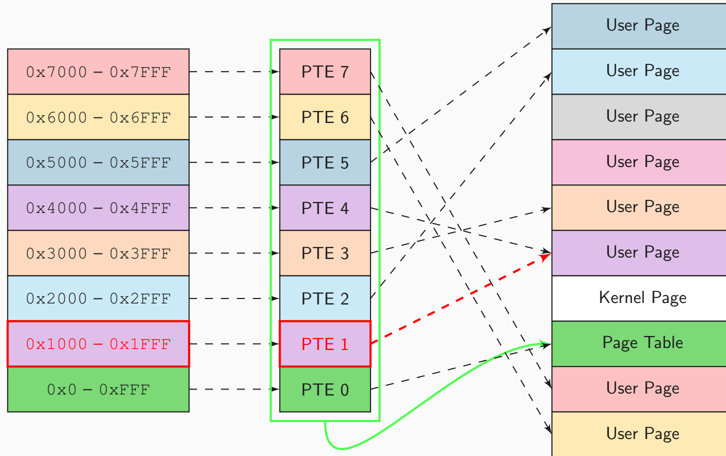
0x6000 – 0x6FFF
0x5000 – 0x5FFF
0x4000 – 0x4FFF
0x3000 – 0x3FFF
0x2000 – 0x2FFF
0x1000 – 0x1FFF
0x0 – 0xFFF
PTE 7
PTE 6
PTE 5
PTE 4
PTE 3
PTE 2
PTE 1
PTE 0
User Page
User Page
User Page
User Page
User Page
User Page
Kernel Page
Page Table
User Page
User Page

Page Table Manipulation



Page Table Manipulation

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0x1000 – 0x1FFF
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PTE 7
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Page Table
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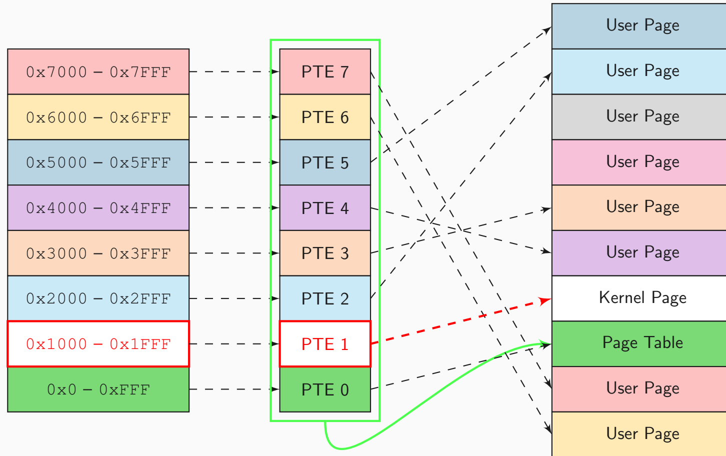
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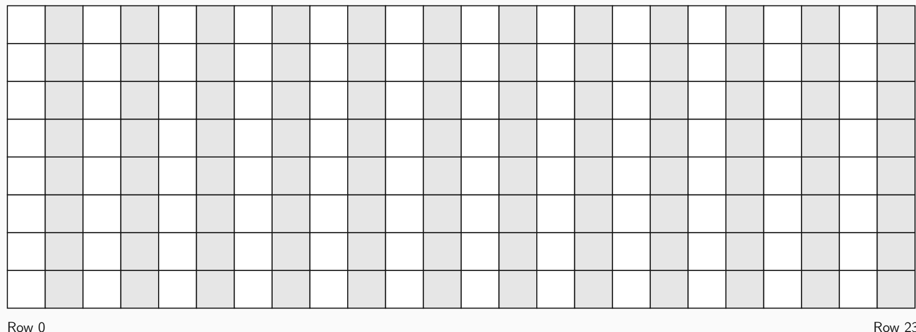
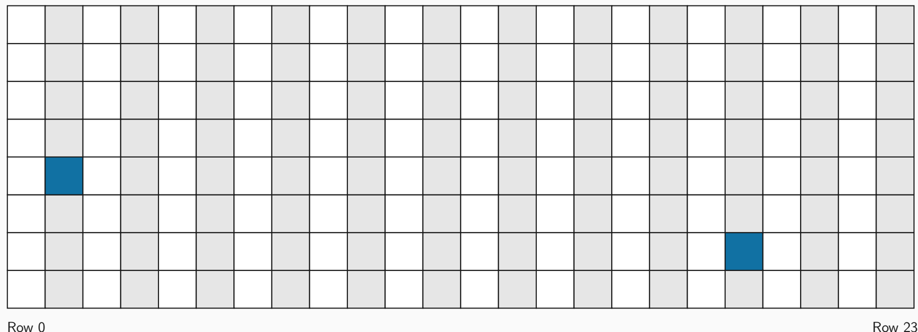
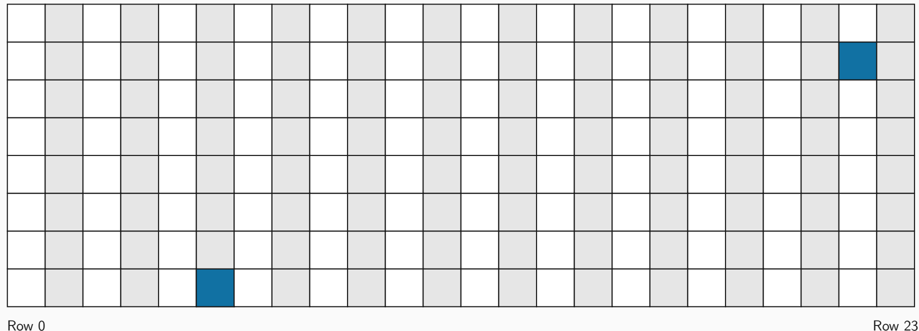


Hammering memory locations in different rows



Hammering memory locations in different rows

Search for page with flip



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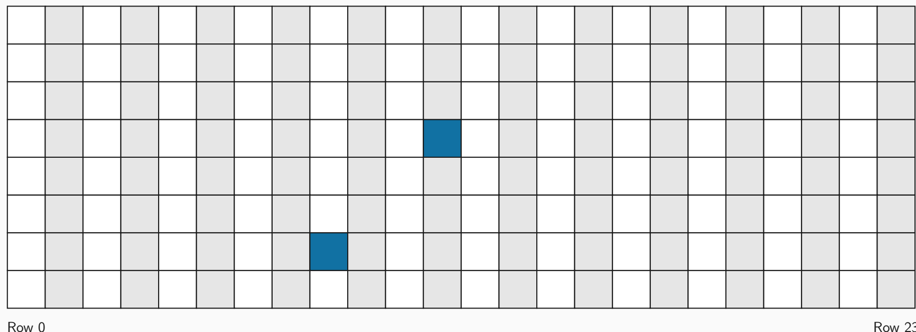

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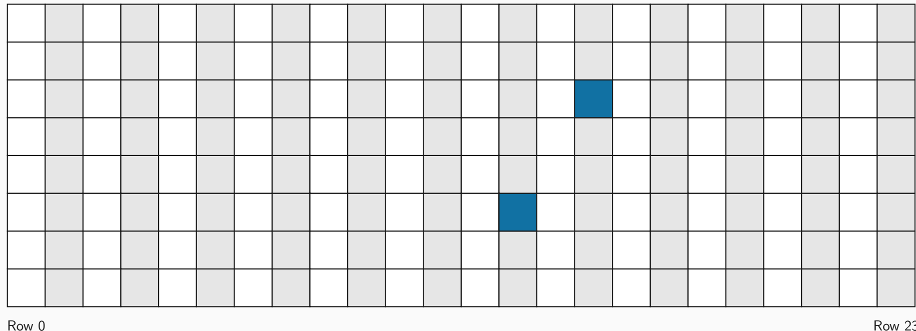

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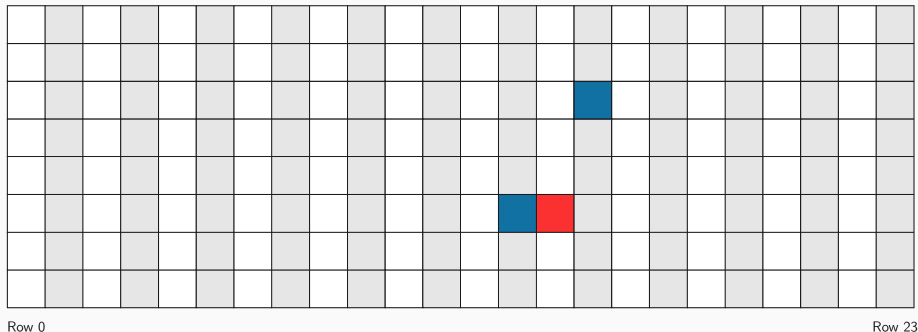
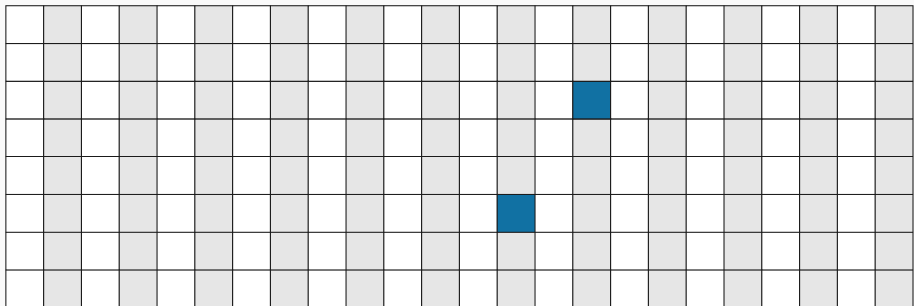


Hammering memory locations in different rows

Fill all remaining memory with page tables



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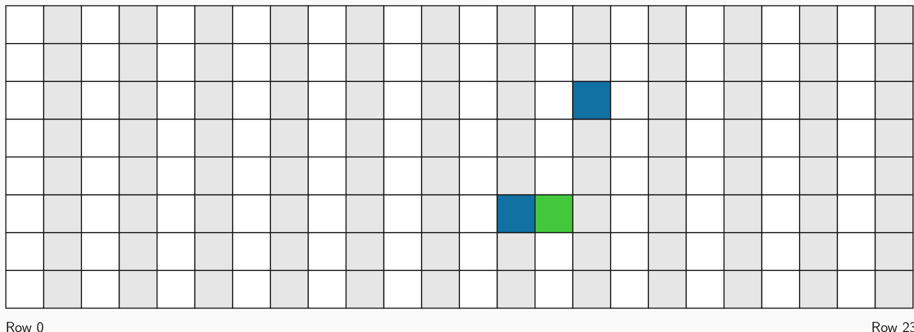

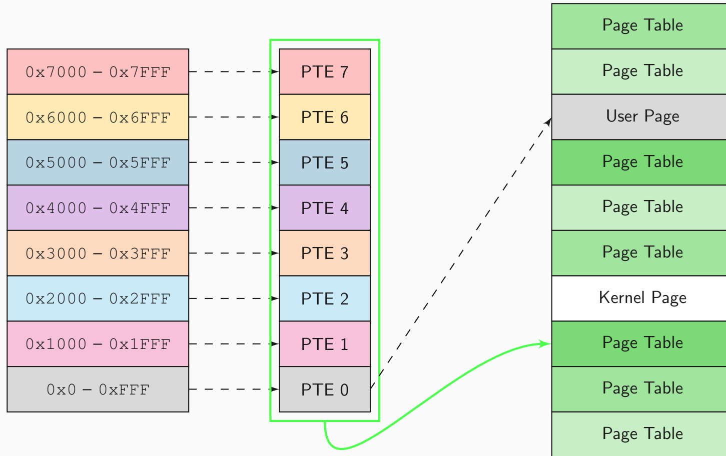

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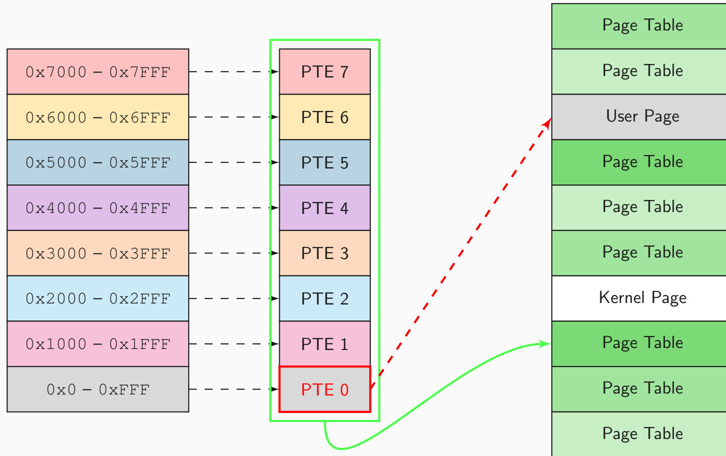

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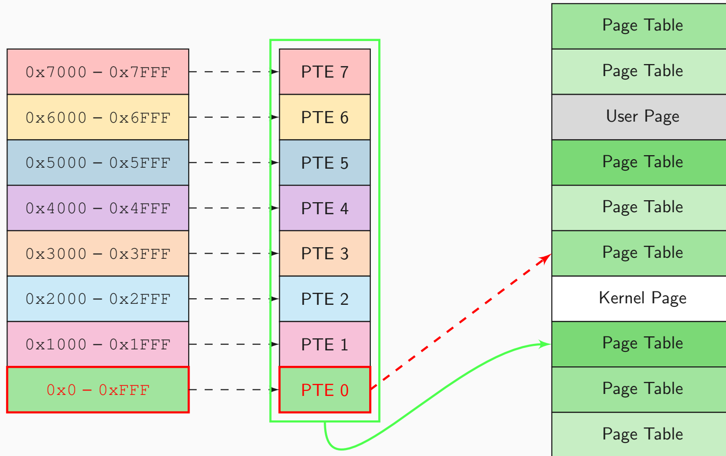

Strategy: Flipping Page Table PPN bits

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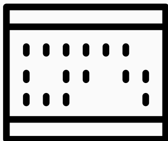

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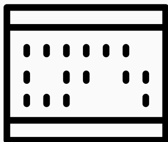

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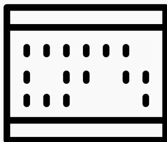

1. Scan for flips

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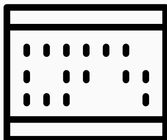

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2. Exhaust or massage memory to place a page table at target location

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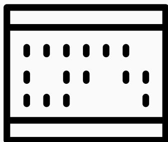
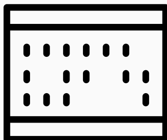


1. Scan for flips
2. Exhaust or massage memory to place a page table at target location
3. Gain access to your own page table → kernel privileges

Flipping Page Table PPN bits



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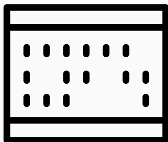
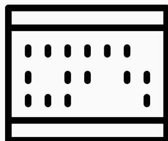
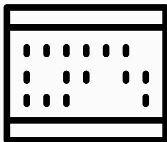


Flipping Page Table PPN bits



- Idea from [31]

Flipping Page Table PPN bits



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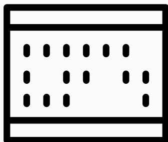
- Same idea applied in several other works:

Flipping Page Table PPN bits



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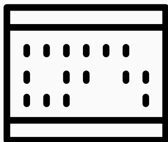

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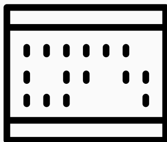
Flipping Page Table PPN bits



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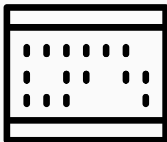

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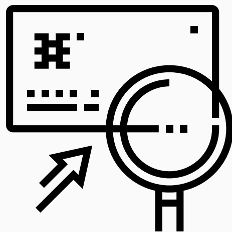
    - Rowhammer.js [13]
    - One bit flips, one cloud flops [35]
    - Drammer [33]
    - Half-Double Rowhammer [21]

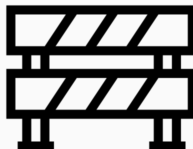
How to mitigate Rowhammer?

Different mitigations have been proposed:



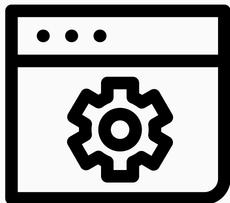
Detection

vs



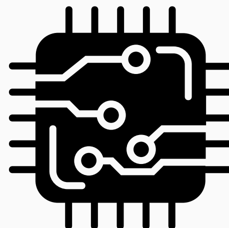
Prevention

Different mitigations have been proposed:



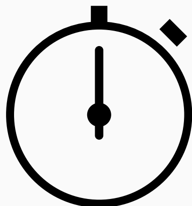
Software

vs



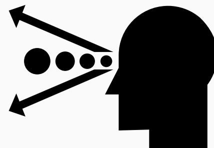
Hardware

Different mitigations have been proposed:



Short Term

vs



Long Term

- No `clflush` instruction

- No `clflush` instruction → Rowhammer.js

Quick fixes

- No `clflush` instruction $\rightarrow$ Rowhammer.js
- Increase the refresh rate

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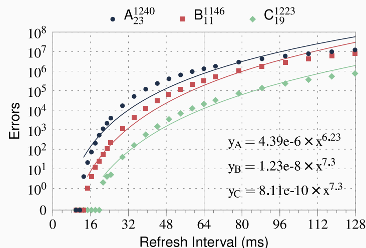
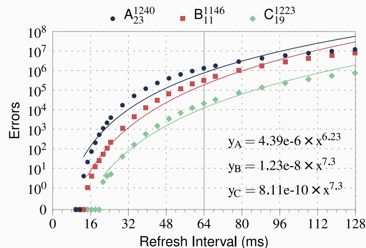
  - → Would need to be increased by 7× to eliminate all bit flips



Errors depending on refresh interval [20]

- No `clflush` instruction → Rowhammer.js
- Increase the refresh rate
  - → Would need to be increased by 7× to eliminate all bit flips
  - → Implementation: increased by 2× by BIOS vendors



Errors depending on refresh interval [20]

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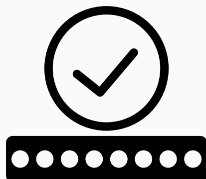

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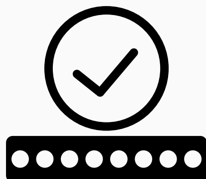

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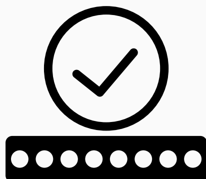

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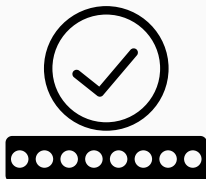

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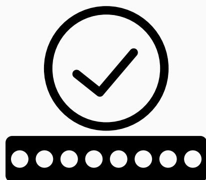

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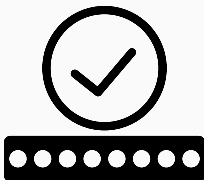

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- ECCploit actively targeting ECC DRAM with Rowhammer [0]

Preventing Rowhammer attacks in hardware

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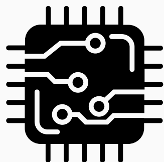
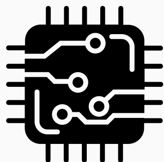
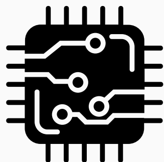


Original ideas from [20]





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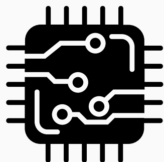

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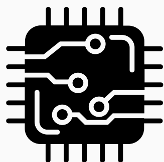

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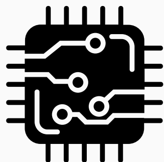

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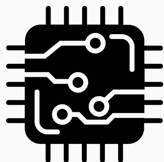

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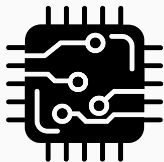

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→ Expensive, performance overhead, or increased power consumption

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- Static analysis of the binary

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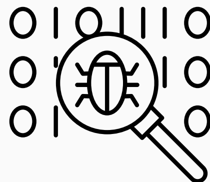

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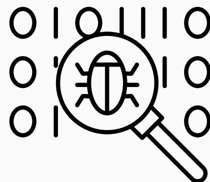
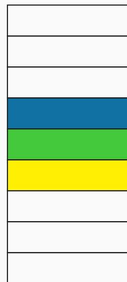
ThrowHammer [32], NetHammer [23].



- B-CATT: disable vulnerable physical memory [5]
- G-CATT: isolate security domains in physical memory based on potential vulnerability [5]



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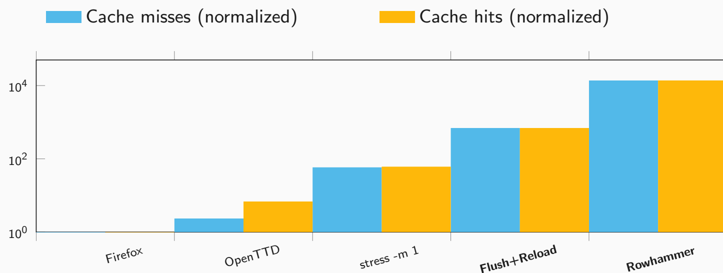
G-CATT: Bit flips more than 8 "rows" apart [12, 20]

- Rowhammer: lots of cache misses that can be monitored with hardware performance counters [7, 14, 15, 24]



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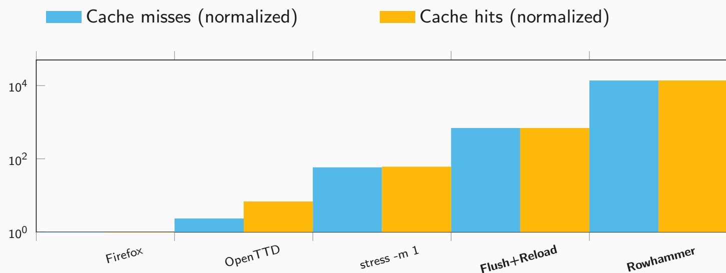
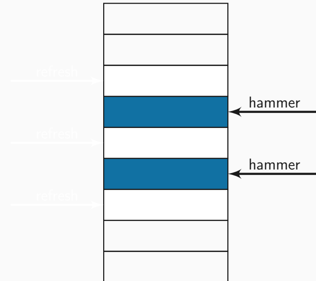
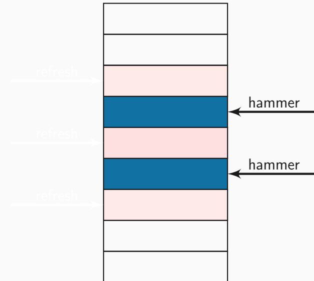


What if performance counters do not work because we run in SGX? [12, 17]

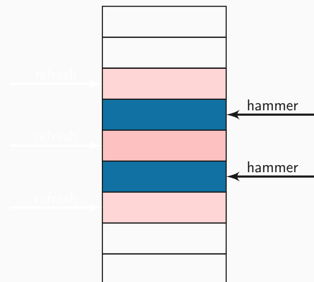
Target Row Refresh (TRR)



- Counter per row



- Counter per row
- Increment neighbor rows



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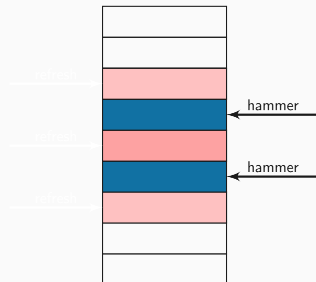

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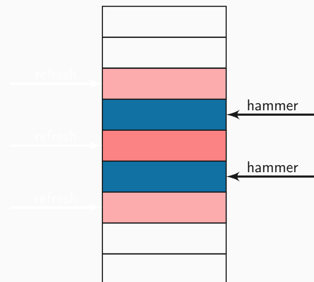

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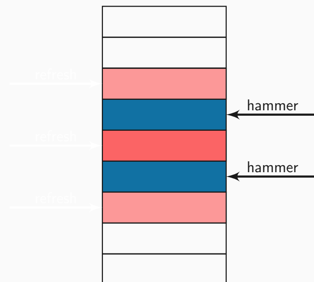

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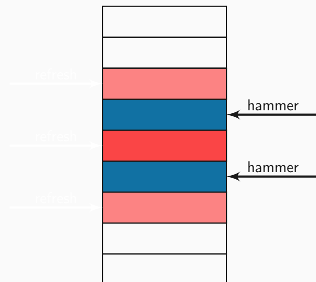

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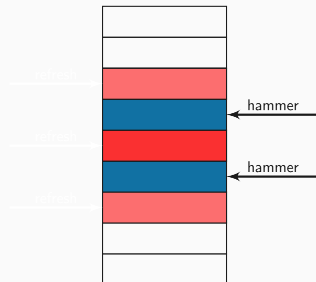

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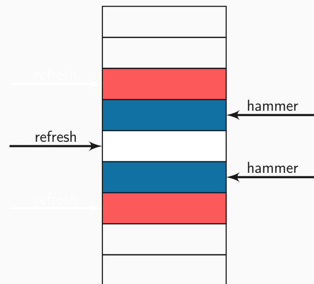

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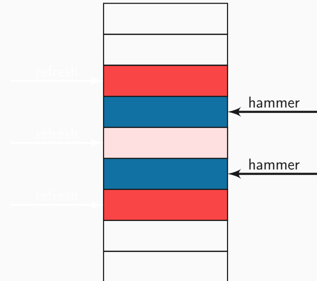

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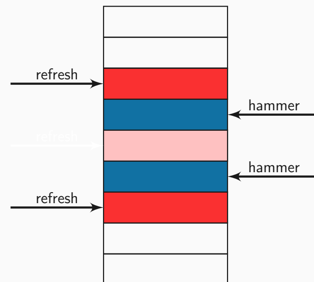

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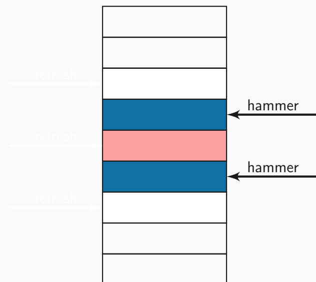

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Defenses Overview

Methodology \ Defense	MASCAT	Chiapetta et al. [7]	CloudRadar	[15]	HexPADS	perf	ANVIL	nohammer	No OOM	G-CATT	B-CATT	TRR	MAC	PARA/CRA/PRA	ARMOR	ECC/Chipkill	Refresh Rate
Detection																	
Static Analysis	●	○	○	◐	○	○	○	○	○	○	○	○	○	○	○	○	○
Performance Counters	○	●	●	●	●	●	●	○	○	○	○	○	○	○	○	○	○
Memory Access Pattern	○	○	○	○	○	○	●	●	○	○	○	○	○	○	○	○	○
Neutralization																	
Physical Proximity	○	○	○	○	○	○	○	○	○	●	○	○	○	○	○	○	○
Memory Footprint	○	○	○	○	○	○	○	○	●	○	○	○	○	○	○	○	○
Elimination																	
Bootloader	○	○	○	○	○	○	○	○	○	○	●	○	○	○	○	○	○
Hardware Modification	○	○	○	○	○	○	○	○	○	○	○	●	●	●	●	●	○
BIOS Update	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	●

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One-location hammering

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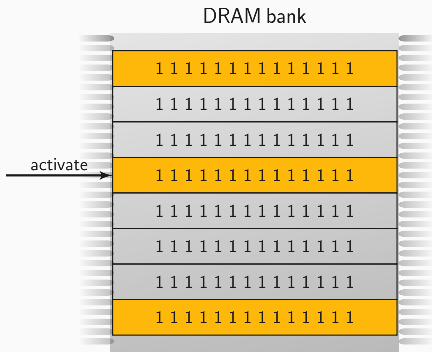

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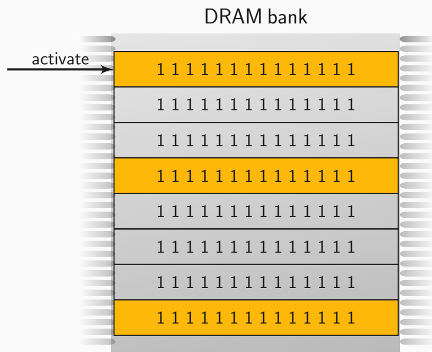

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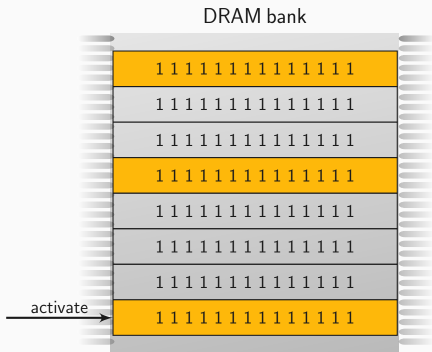

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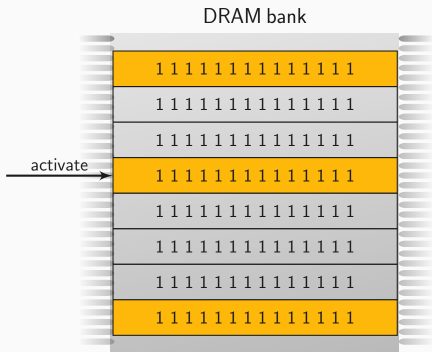

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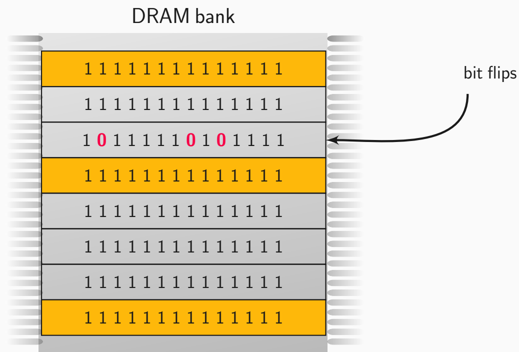

#2 - Double-sided hammering

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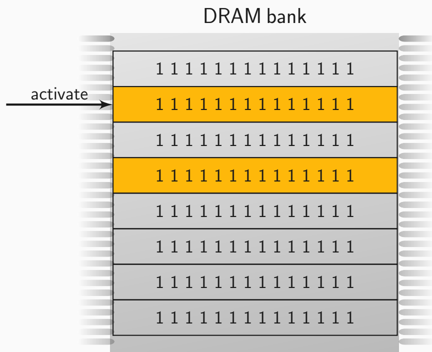

#2 - Double-sided hammering

DRAM bank

activate

1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
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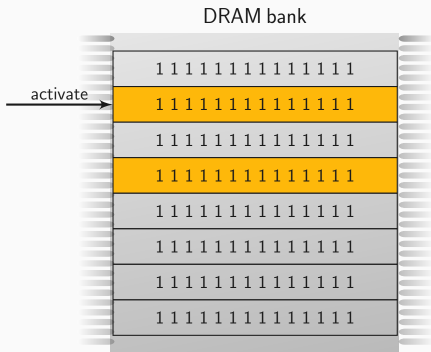
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1 1 1 1 1 1 1 1 1 1 1 1 1 1
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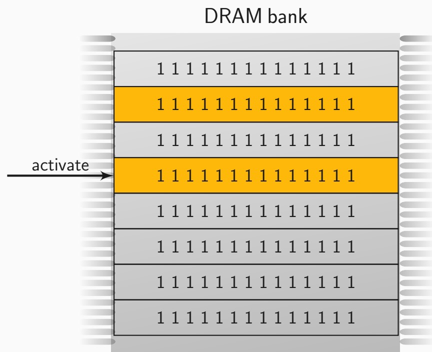

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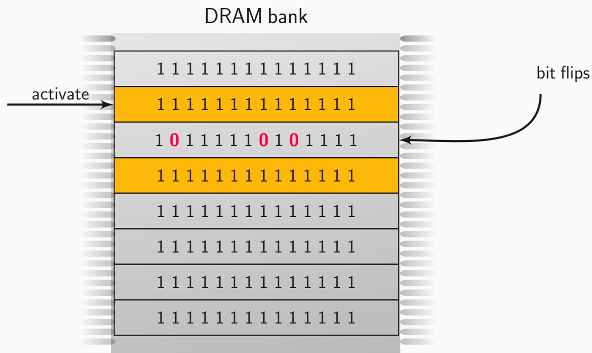
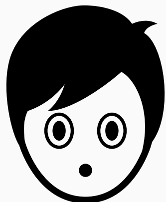


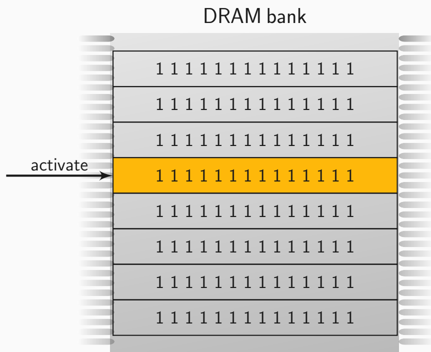
HAMMERING
TWO ROWS

HAMMERING TWO ROWS

HAMMERING A SINGLE ROW



- There are three different hammering techniques
- #1: Hammer one row next to victim row and other random rows
- #2: Hammer two rows neighboring victim row
- #3: Hammer only one row next to victim row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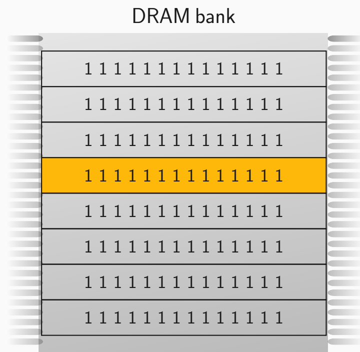
#3 - One-location hammering / Rowpress



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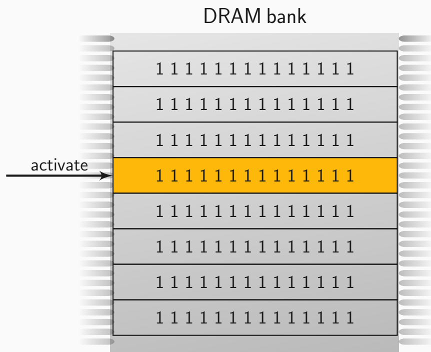
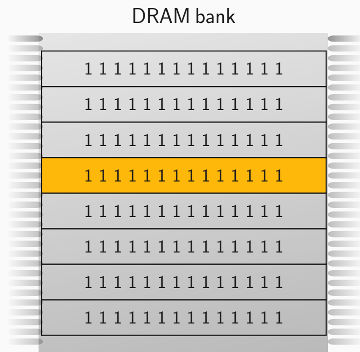
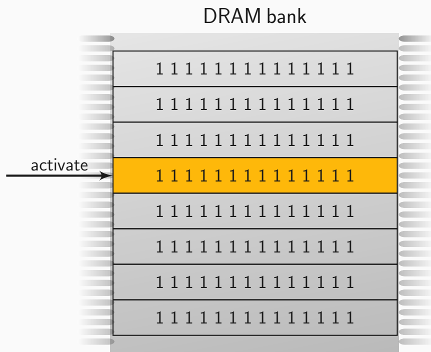
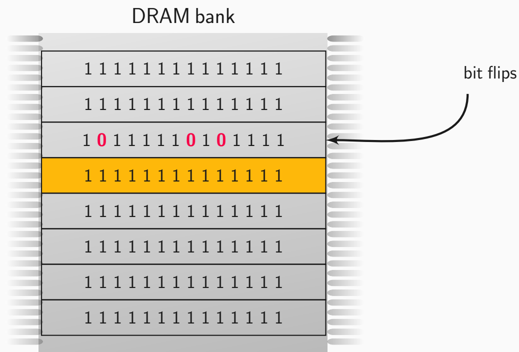


#3 - One-location hammering / Rowpress



#3 - One-location hammering / Rowpress




DRAM bank
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 0 1 1 1 1 1 0 1 0 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1
bit flips

dgruss@lab05: ./rowhammer 13

File Edit View Search Terminal Help

```
dgruss@lab05 ~/flipfloyd (git)-[master] % make
g++ -std=c++11 -O3 -o rowhammer rowhammer.cc
dgruss@lab05 ~/flipfloyd (git)-[master] % ./rowhammer 13
Allocating memory... 90%
```

Two underlying reasons:

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- Memory-controller page policies

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Two underlying reasons:

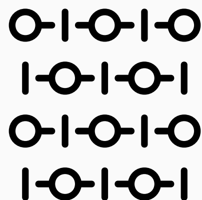
- Memory-controller page policies
- Physical effect called RAS-clobber

Two underlying reasons:

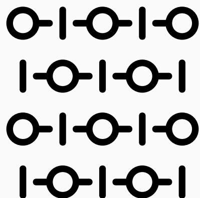
- Memory-controller page policies

- Physical effect called RAS-clobber
- Recently shown in Rowpress paper [0]

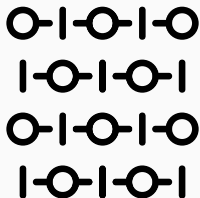
Memory-Controller Policies



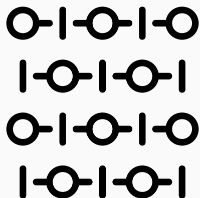
- **Open-page policy**: Keep row opened and buffered



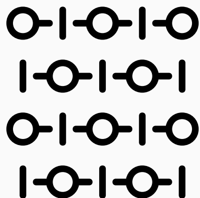
- **Open-page policy**: Keep row opened and buffered
  - Low latency for subsequent accesses to same row
  - High latency for accesses to any other row



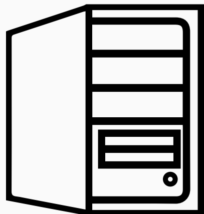
- **Open-page policy**: Keep row opened and buffered
  - Low latency for subsequent accesses to same row
  - High latency for accesses to any other row
- **Closed-page policy**: Immediately close row, ready to open a new row



- **Open-page policy**: Keep row opened and buffered
  - Low latency for subsequent accesses to same row
  - High latency for accesses to any other row
- **Closed-page policy**: Immediately close row, ready to open a new row
  - Medium latency for accesses to any row

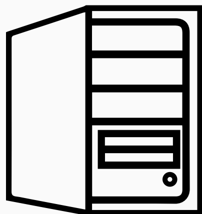


- **Open-page policy**: Keep row opened and buffered
  - Low latency for subsequent accesses to same row
  - High latency for accesses to any other row
- **Closed-page policy**: Immediately close row, ready to open a new row
  - Medium latency for accesses to any row
  - Perform better on multi-core systems [9]

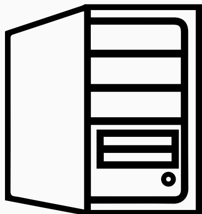


- Policies that preemptively close rows, would allow one-location hammering

Memory-Controller Policies

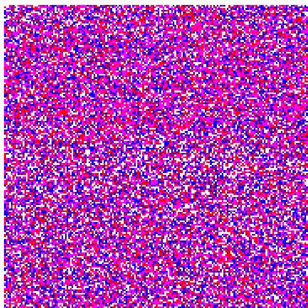


- Policies that preemptively close rows, would allow one-location hammering
- We observed close-page policies on desktop computers



- Policies that preemptively close rows, would allow one-location hammering
- We observed close-page policies on desktop computers
- Mobile devices (e.g., laptops) seem to use mostly open-page policies

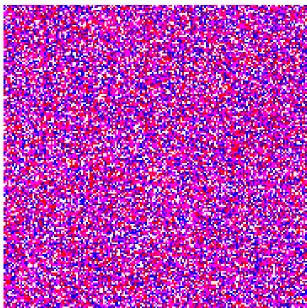
How well does it work?



Double-sided

77.0 % bit offsets

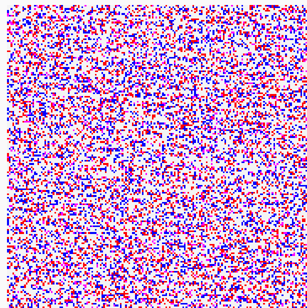
51.7 % 0→1 bit flips



Single-sided

78.5 % bit offsets

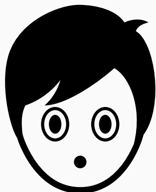
54.1 % 0→1 bit flips



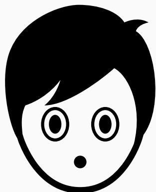
One-location

36.5 % bit offsets

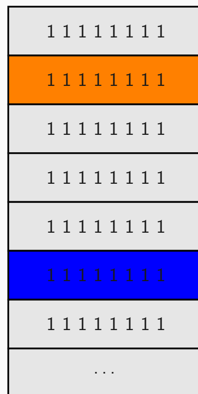
51.6 % 0→1 bit flips



- There are four different hammering techniques
- #1: Hammer one row next to victim row and other random rows
- #2: Hammer two rows neighboring victim row
- #3: Hammer only one row next to victim row



- There are four different hammering techniques
- #1: Hammer one row next to victim row and other random rows
- #2: Hammer two rows neighboring victim row
- #3: Hammer only one row next to victim row
- #4: Hammer from a larger distance with the **help** of TRR [21]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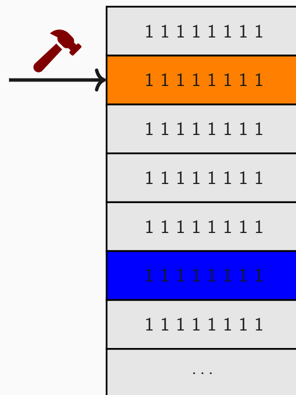
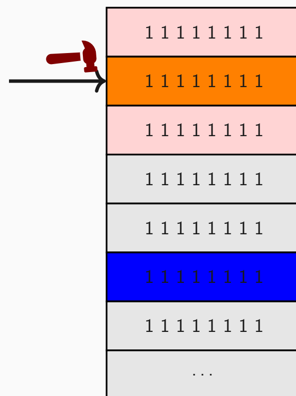
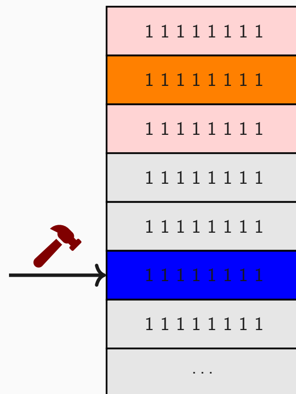
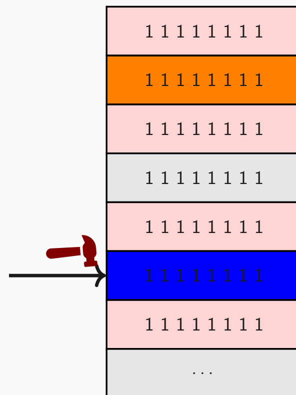
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
. . .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1 1 1 1 1 1 1 1
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1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
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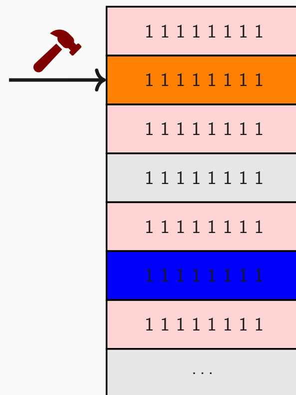
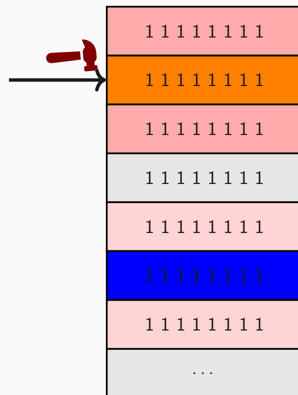
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
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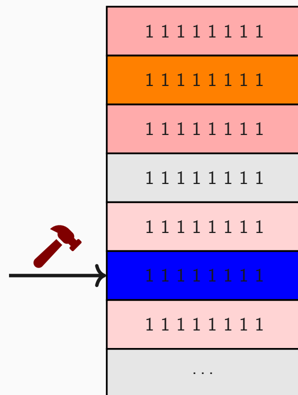
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
. . .


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
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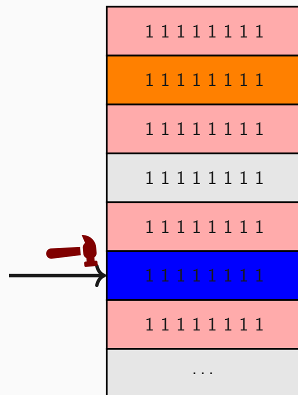
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
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1 1 1 1 1 1 1 1
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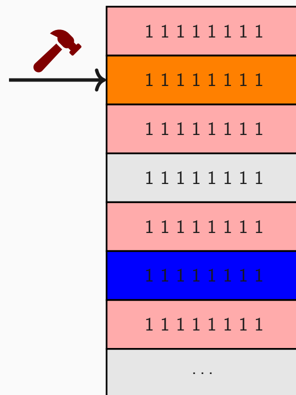
1 1 1 1 1 1 1 1
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1 1 1 1 1 1 1 1
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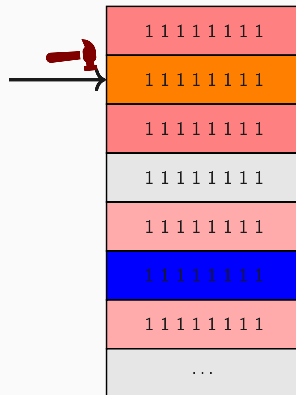
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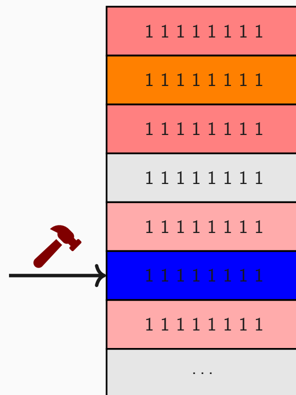
...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1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
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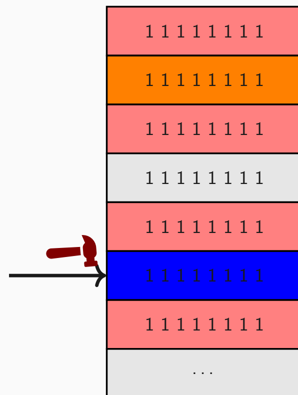
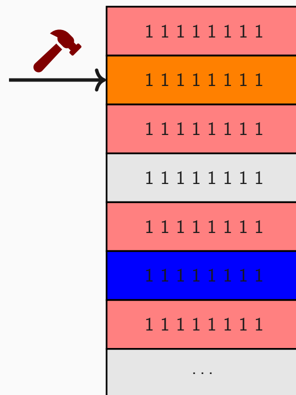
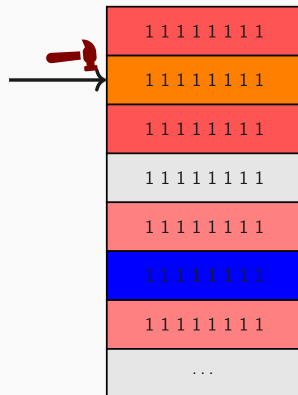
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...

Half-Double Rowhammer




1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
. . .


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
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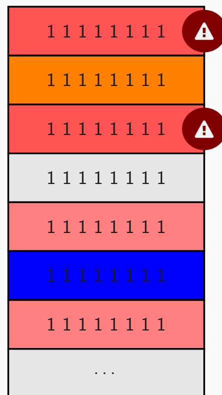
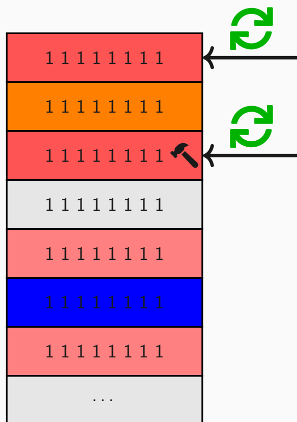
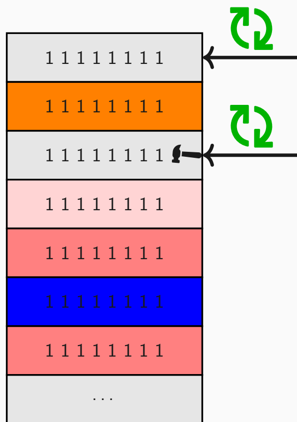
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...

Half-Double Rowhammer

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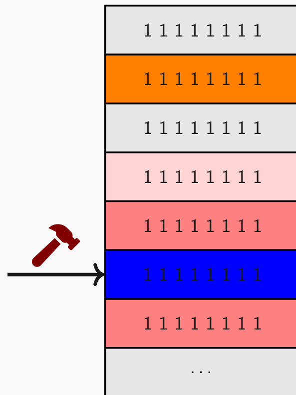
...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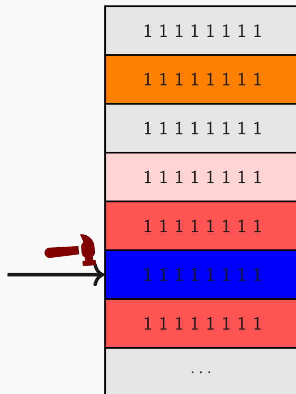
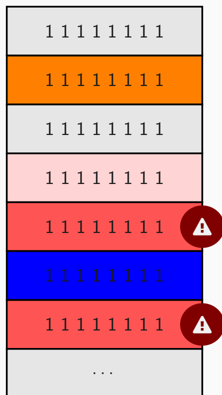
. . .

Half-Double Rowhammer





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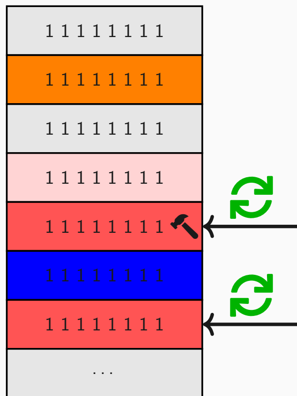
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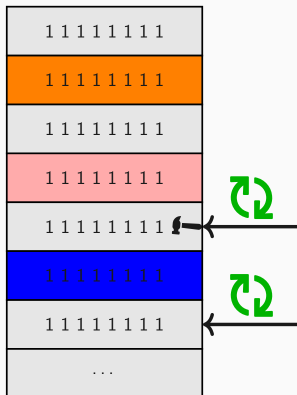
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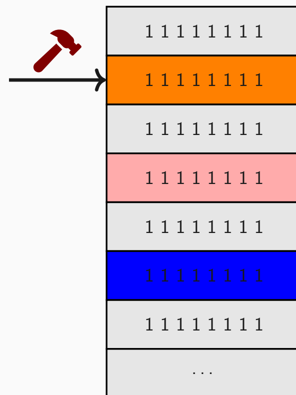
. . .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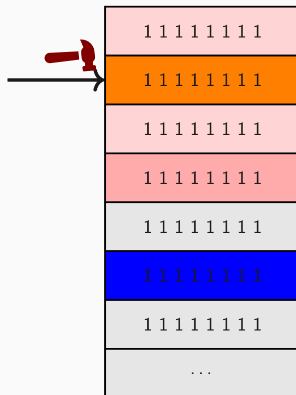
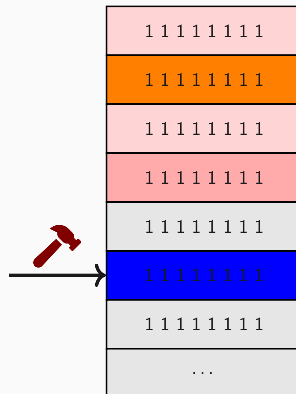
Half-Double Rowhammer

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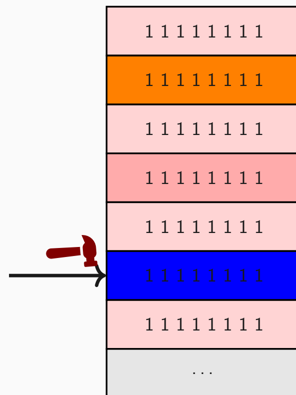
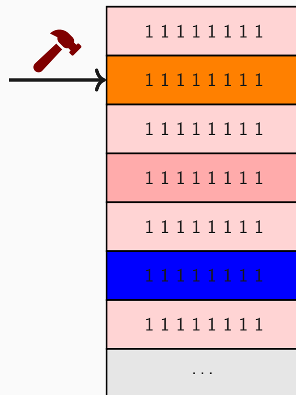
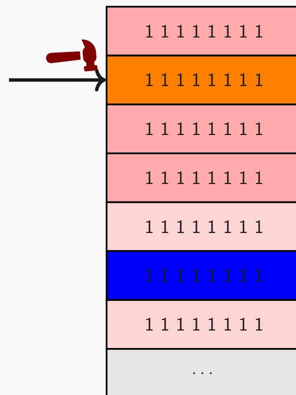
1 1 1 1 1 1 1 1
...

Half-Double Rowhammer



Half-Double Rowhammer

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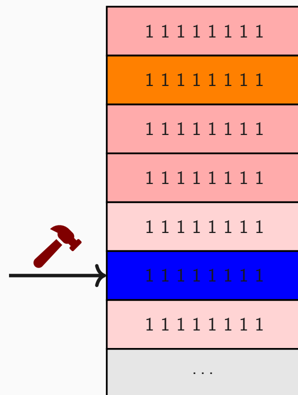
1 1 1 1 1 1 1 1
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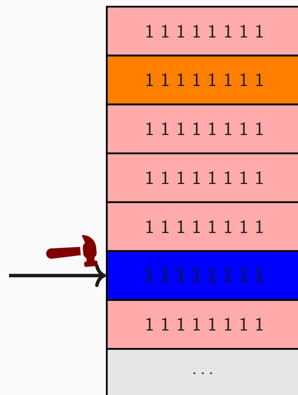
...


1 1 1 1 1 1 1 1
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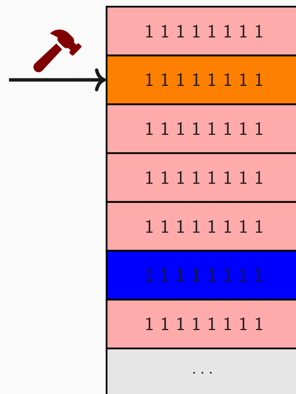
...


1 1 1 1 1 1 1 1
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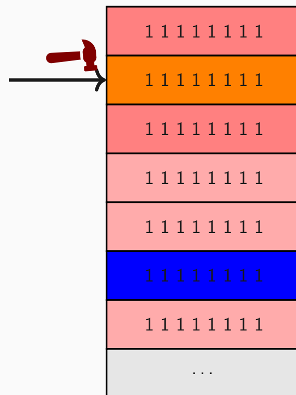
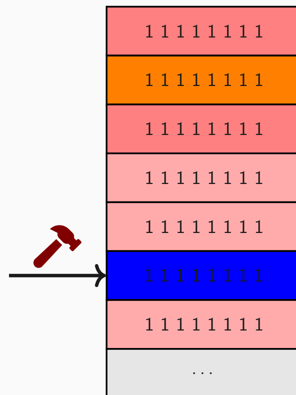
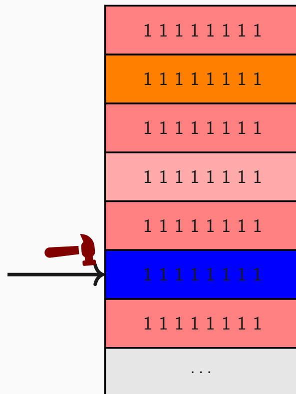
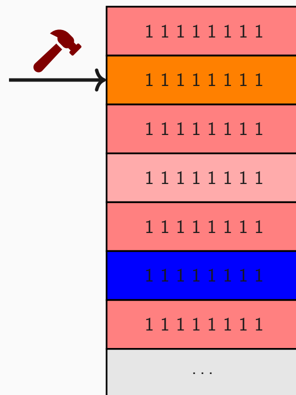
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...

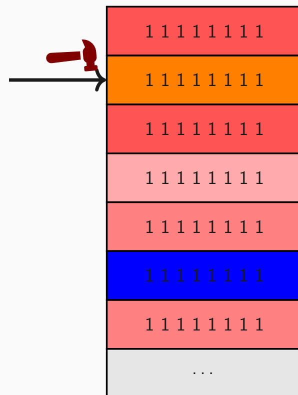

1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
. . .

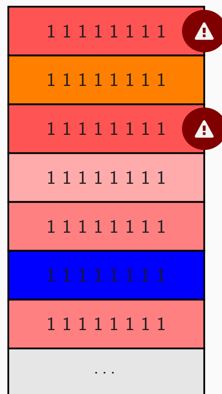

1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...

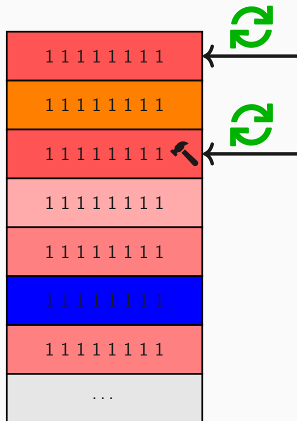

1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...

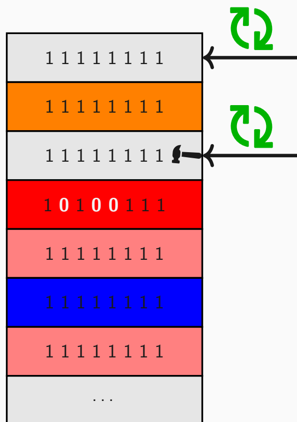
Half-Double Rowhammer

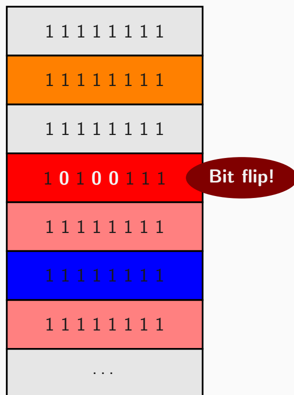



1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
. . .


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 0 1 0 0 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...


1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 0 1 0 0 1 1 1
Bit flip!
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1
...

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- Developing countermeasures for a such a problem is **hard**

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- Target `sudo` (easy to exploit)

JE
HLT
0 1 1 1 0 1 0 0
1 1 1 1 0 1 0 0

Opcode Flipping - Conditional Jump

JE
0 1 1 1 0 1 0 0
PUSHQ
0 1 0 1 0 1 0 0

Opcode Flipping - Conditional Jump

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JE
0 1 1 1 0 1 0 0
JO
0 1 1 1 0 0 0 0

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- They all somehow skipped the password check

How to get the target virtual page to the target physical location?

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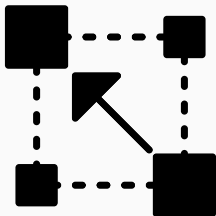
Memory Waylaying

Placing the binary



- Not as easy as with page tables

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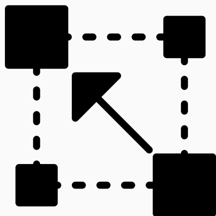

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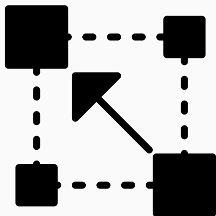

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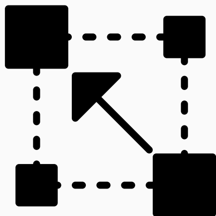
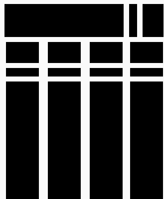
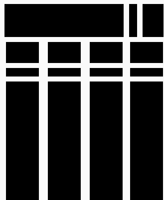


- Not as easy as with page tables
- Binary only once in memory + stays in memory (in the page cache) even after termination
- Only evicted if page cache is full
- Page cache usually occupies all unused memory



- If a binary is loaded the first time, it is loaded to the memory



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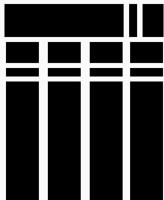
Page Cache



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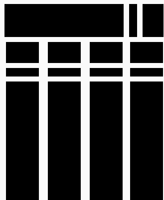
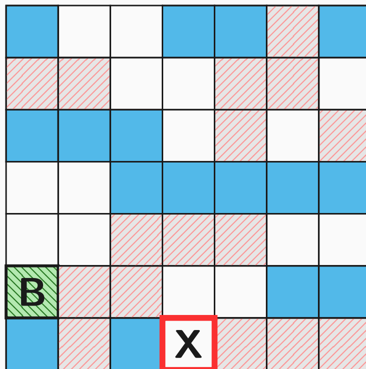


- If a binary is loaded the first time, it is loaded to the memory
- It stays in memory (in the page cache) even after execution
- Only evicted if page cache is full
- Page cache is huge - usually all unused memory

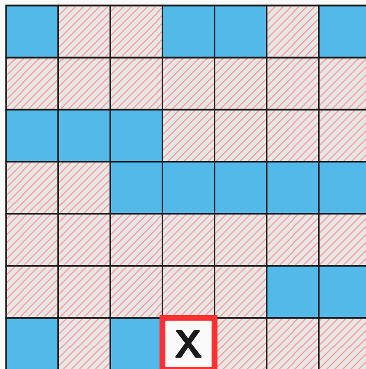
MEMORY WAYLAYING

Wait for the right moment, and then hit it with a bit flip!

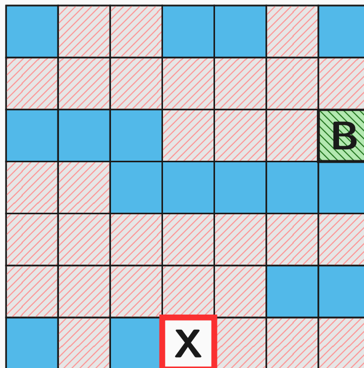
(1) Start



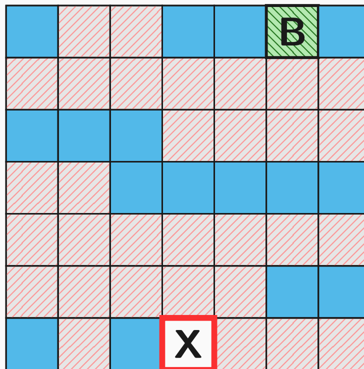
(2) Evict Page Cache



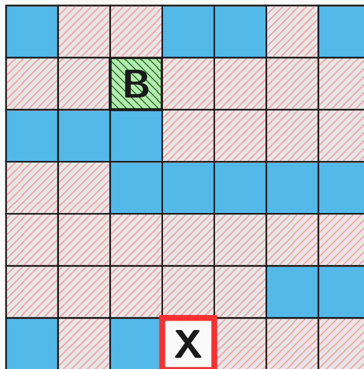
(3) Access Binary



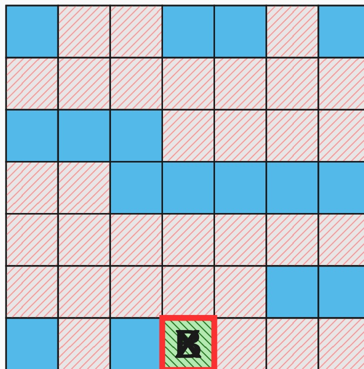
(4) Evict + Access



(5) Evict + Access

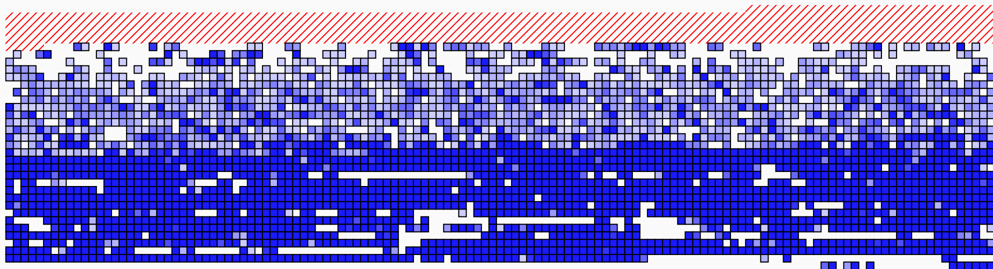


(6) Stop if target reached

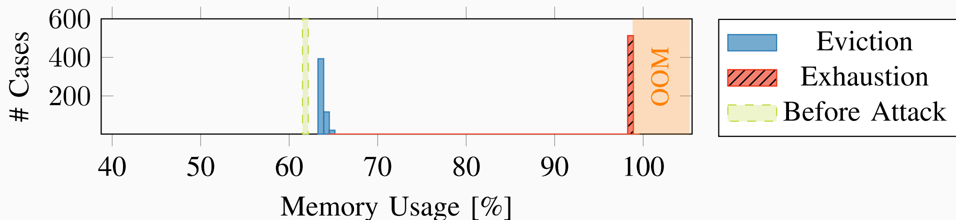


How well does it work?

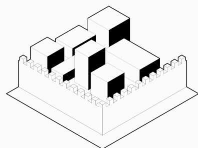
- New pages cover most of the physical memory



- Great advantage over memory massaging: only negligible memory footprint

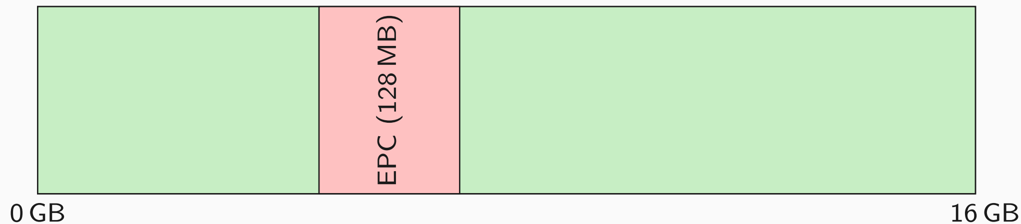


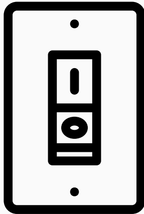
Rowhammer + SGX = Cheap Denial of Service



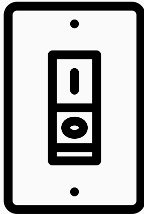
- Instruction-set extension
- Integrity and confidentiality of code and data in untrusted environments
- Run with user privileges and restricted, e.g., no system calls
- Run programs in enclaves using protected areas of memory

0 GB
16 GB


EPC (128 MB)
0 GB
16 GB



- What happens if a bit flips in the EPC?



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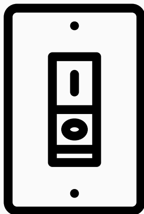
- Integrity check will fail!



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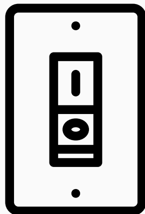
→ Locks up the memory controller



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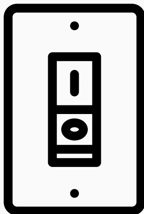

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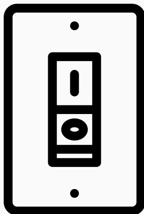
→ System halts immediately



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SOUNDS UNSAFE?
IT IS UNSAFE!
imgflip.com

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- . . . the entire machine halts

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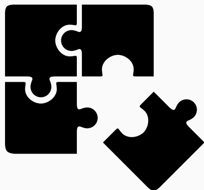
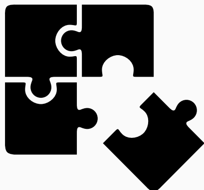
- Denial-of-Service Attacks in the Cloud [12, 17]

SGX + One-location Hammering + Opcode Flipping = Undetectable Exploit



- SGX protects software from malicious environments



- SGX protects software from malicious environments
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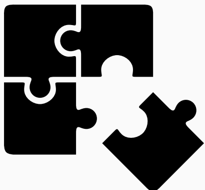
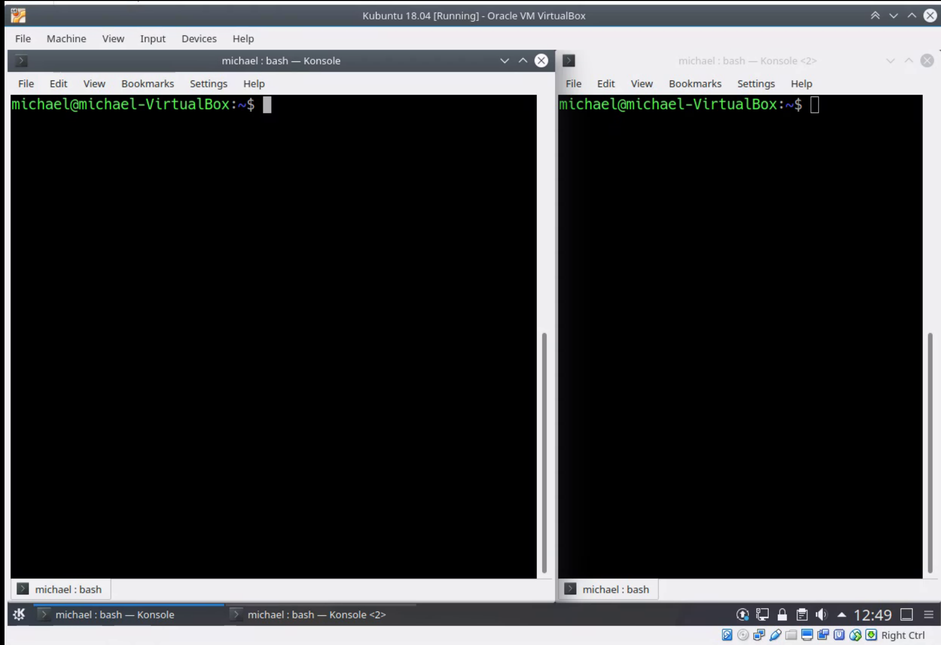
(Ab)using SGX Protection

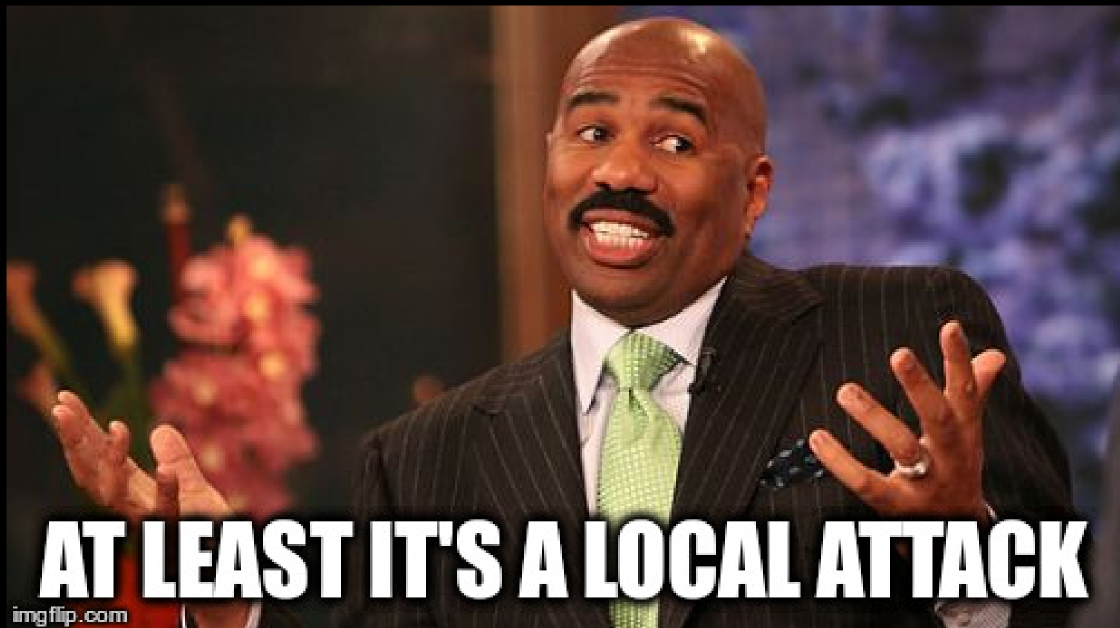


- SGX protects software from malicious environments
- Thwarts static and dynamic (= performance counters) analysis
- Hammering from SGX defeats countermeasures relying on this

STEALTH LEVEL: EXPERT


Kubuntu 18.04 [Running] - Oracle VM VirtualBox
File Machine View Input Devices Help
michael : bash — Konsole
File Edit View Bookmarks Settings Help
michael@michael-VirtualBox:~$
michael : bash
michael : bash — Konsole <2>
File Edit View Bookmarks Settings Help
michael@michael-VirtualBox:~$
michael : bash
michael : bash — Konsole
michael : bash — Konsole <2>
12:49
Right Ctrl

Bypass \ Defense Class	Static Analysis	Performance Counters	Memory Access Pattern	Physical Proximity	Memory footprint
Intel SGX	●	●	○	○	○
One-location hammering	○	○	●	○	○
Opcode flipping	○	○	○	●	○
Memory waylaying	○	○	○	○	●
Defense class defeated	●	●	●	●	●


AT LEAST IT'S A LOCAL ATTACK
imgflip.com

Just comparing some performance numbers...

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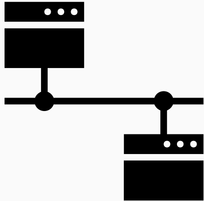
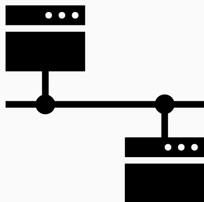
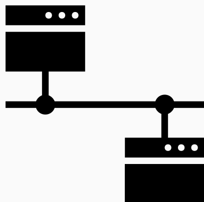


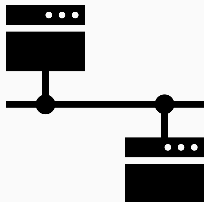


Inducing bit flips:



Inducing bit flips:

- Network stacks on ARM often use uncached memory (perfect for hammering)



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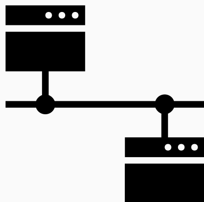
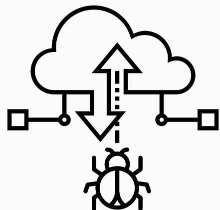
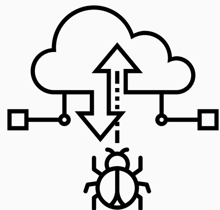


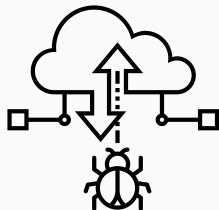
Inducing bit flips:

- Network stacks on ARM often use uncached memory (perfect for hammering)
- Intel recommends Intel CAT for QoS (perfect for hammering)
- Network reachable code might use `clflush` or non-temporal stores
  (both great for hammering)



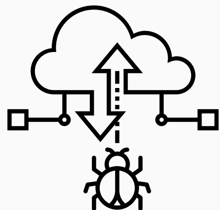


Nethammer on ...



Nethammer on ...

- SGX = powerful DoS



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- SGX = powerful DoS
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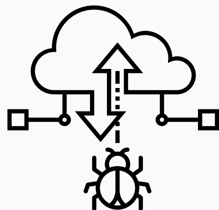

Nethammer on ...

- SGX = powerful DoS
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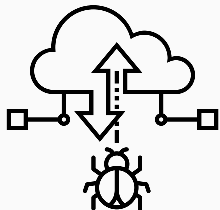
Exploiting Nethammer Bit Flips



Nethammer on ...

- SGX = powerful DoS
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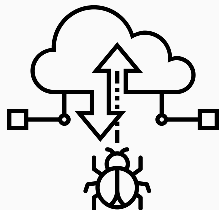
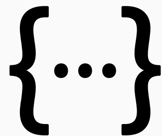
- OCSP servers = make invalid certificates great again



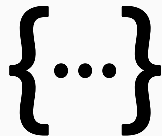
Nethammer on ...

- SGX = powerful DoS
- File system = persistent DoS
- DNS entries on a DNS server = bit-squatting attack
- OCSP servers = make invalid certificates great again
- Crypto = generate private keys for broken public keys



- Many (academic) countermeasures were proposed to mitigate Rowhammer

What do we learn from it?



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- We showed that all of them can be circumvented [12]

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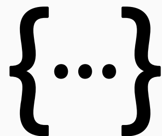

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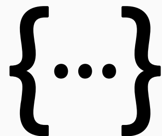
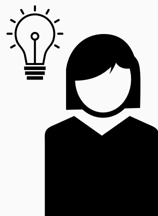
- We cannot design countermeasures focused on specifics of the attack



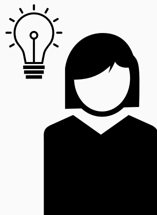
- Many (academic) countermeasures were proposed to mitigate Rowhammer
- We showed that all of them can be circumvented [12]
- We cannot design countermeasures focused on specifics of the attack
- Otherwise we only patch concrete exploits, but do not solve the problem

What do we learn from it?



Apple had a great idea:

- Lower refresh rate $\rightarrow$ save energy $+$ more flips



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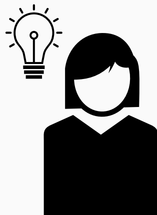

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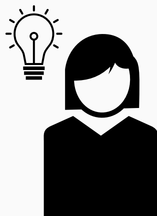

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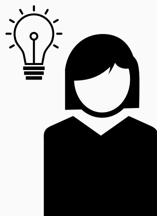

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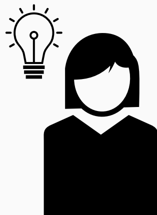

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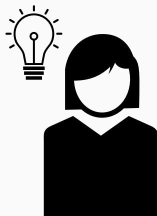

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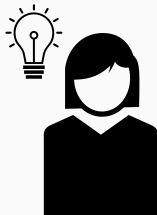

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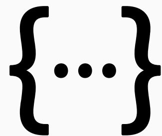
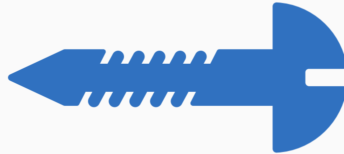
  → Difficult to optimize with an adversary working against you

A new Era of Rowhammer Countermeasures?

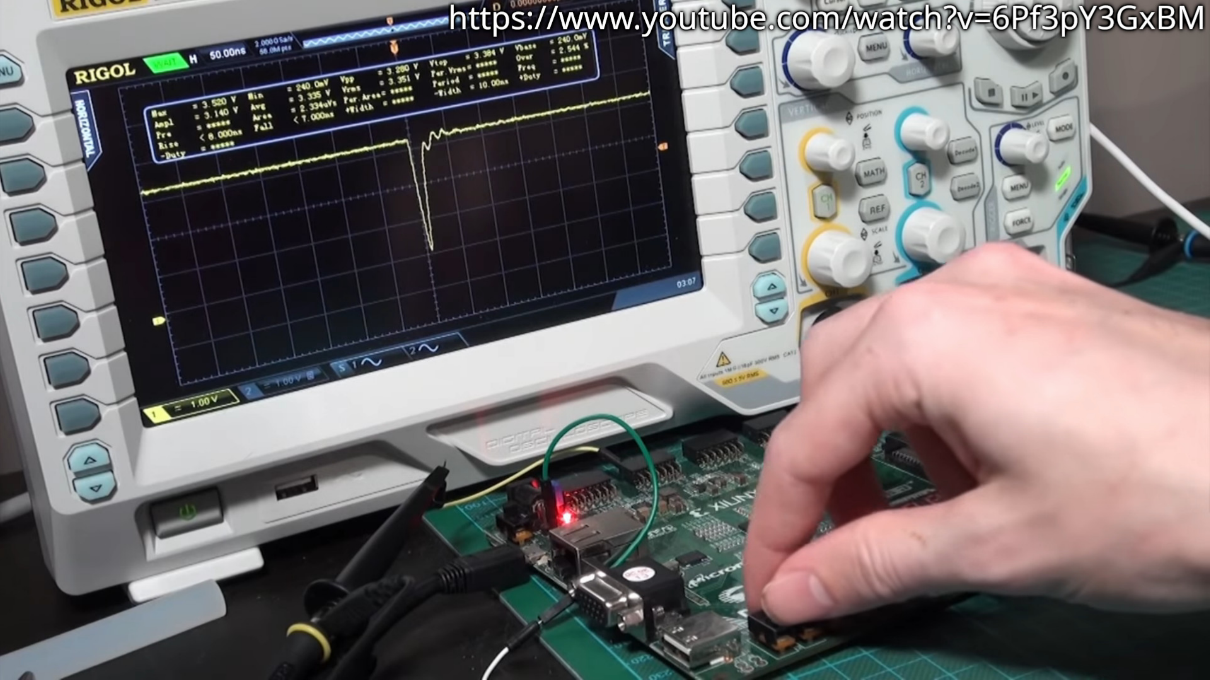


- Data integrity protection for **all data** in the DRAM [19]
- Compute Cryptographic MAC on all data
- No focus on Rowhammer
- No new hammer method or exploit can circumvent it

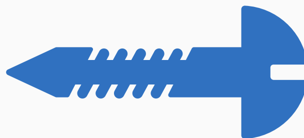
Anything other than Rowhammer?



A NEW CLASS OF FAULT ATTACKS


https://www.youtube.com/watch?v=6Pf3pY3GxBM
RIGOL
50.00ns
MENU
MATH
REF
FORCE
03:07
1.00 V

Our starting point...



Tang2017

DVFS

Changing the voltage and frequency of the CPU

Changing the voltage and frequency of the CPU

- Gamers want fast responses

Changing the voltage and frequency of the CPU

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- Cloud servers want high-assurance and low running costs

Dynamic Voltage and Frequency Scaling

Changing the voltage and frequency of the CPU

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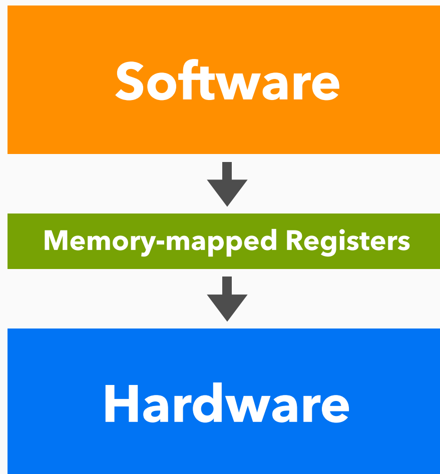
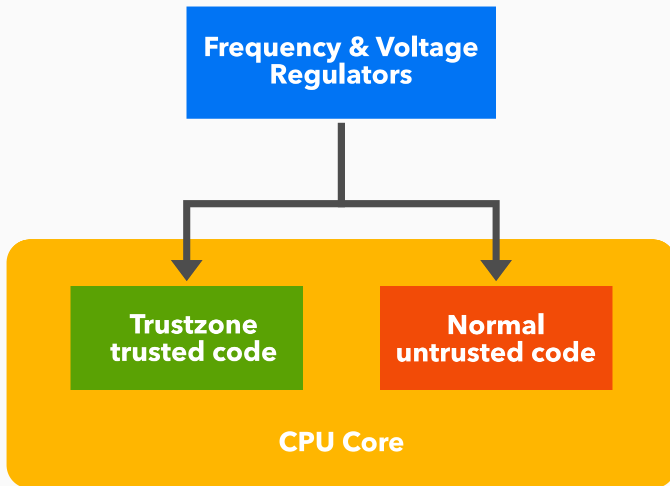
- What if the hardware gets hot?

Dynamic Voltage and Frequency Scaling

Changing the voltage and frequency of the CPU

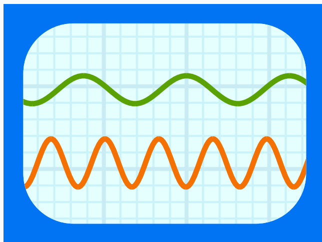
- Gamers want fast responses
- Cloud servers want high-assurance and low running costs
- What if the hardware gets hot?
- Optimal voltage & frequency is difficult!


Software
Memory-mapped Registers
Hardware

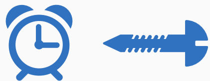


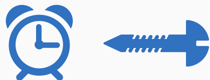
Frequency & Voltage Regulators
Trustzone trusted code
Normal untrusted code
CPU Core

```
add.w    (a0)+,d1
cmp.l    a0,d0
bcc.s    loop
movea.l  #$18E,a1
cmp.w    (a1),d1
bne.w    WrongChecksum
```

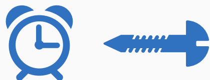


2 + 2 = 5

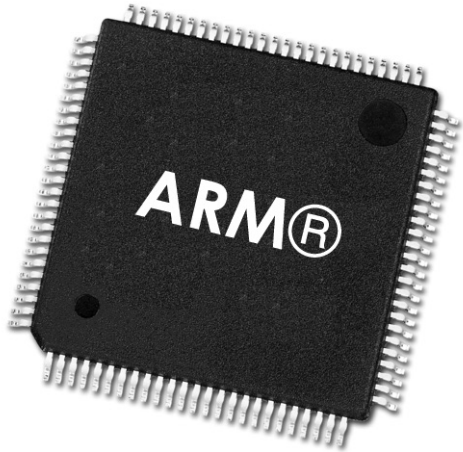




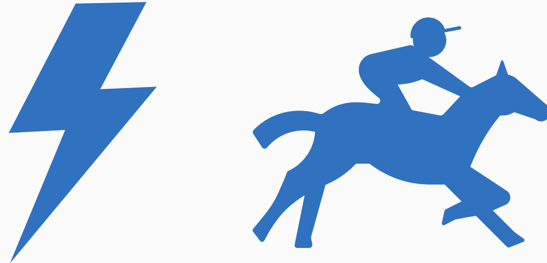
- Infer secret AES key that was stored within Trustzone



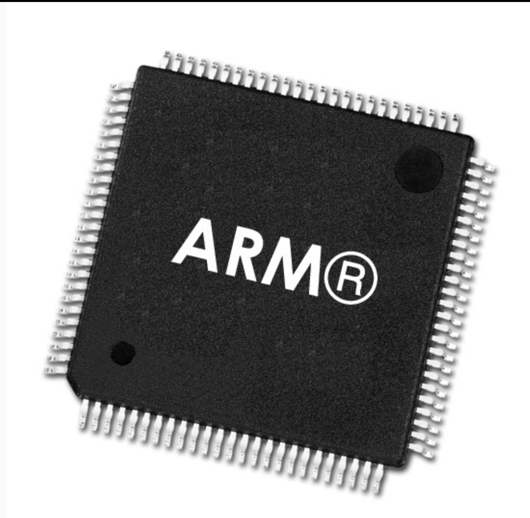
- Infer secret AES key that was stored within Trustzone
- Trick Trustzone into loading a self-signed app


ARM®

More are joining the revolution...

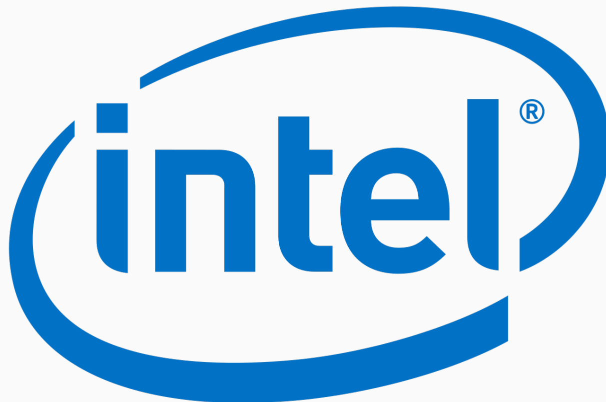


Qiu2019


ARM®

ARE WE ALL THINKING THE SAME THING?

What about Intel?



Intel® Extreme Tuning Utility

Monitoring Settings Help

System Information
Manual Tuning
• All Controls
Core
Graphics
Stress Test
Profiles

Core

Reference Clock 103,2258 MHz
Max Non Turbo Boost Ratio 34 x
Turbo Boost Short Power Max Enable: Disable / Enable
Turbo Boost Short Power Max 1200,000 W
Turbo Boost Power Max 1050,000 W
Turbo Boost Power Time Window 0,00097656 Seconds
Core Current Limit 300,000 A
Additional Turbo Voltage 0,00000 mV

Multipliers

1 Active Core	42 x
2 Active Cores	42 x
3 Active Cores	42 x
4 Active Cores	42 x

4 Active Cores
Default 38 x
Active 38 x
Proposed 42 x
Limits the maximum ratio that the processor can use while four cores are active.

Graphics

Processor Graphics Current Limit 300,000 A

Core	Default	Proposed
Reference Clock	101,0526 MHz	103,2258 MHz
Max Non Turbo Boost Ratio	34 x	34 x
Max Non-Turbo Boost CPU Sp...	3,436 GHz	3,510 GHz
Max Turbo Boost CPU Speed	4,042 GHz	4,335 GHz
1 Active Core	40 x	42 x
2 Active Cores	40 x	42 x
3 Active Cores	39 x	42 x
4 Active Cores	38 x	42 x
Turbo Boost Power Max	1000,000 W	1050,000 W
Turbo Boost Short Power Max	1200,000 W	1200,000 W
Turbo Boost Short Power Max...	Enable	Enable
Turbo Boost Power Time Wind...	0,00097656 S...	0,00097656 S...
Core Current Limit	300,000 A	300,000 A
Additional Turbo Voltage	0,00000 mV	0,00000 mV

Graphics	Default	Proposed
Processor Graphics Current Li...	300,000 A	300,000 A

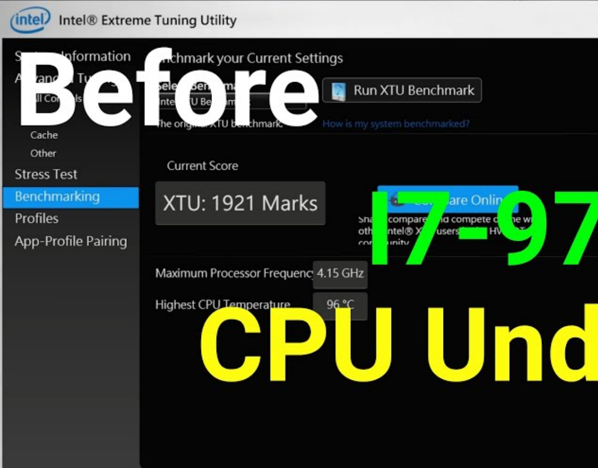
Apply Discard Save to Profile
Force Reboot

CPU Core Temperature 37 °C
CPU Utilization 3 %
Processor Frequency 3,54 GHz
Memory Utilization 2708 MB
CPU Total TDP 15 W

5 Minutes

CPU Utilization 3 %	Memory Utilization 2708 MB	CPU Core Temperature 36 °C	CPU Throttling 0%	Processor Frequency 3,54 GHz
Graphics Frequency 354 MHz	Active Core Count 1	CPU Total TDP 16 W	IACore TDP 10 W	Graphics TDP 0 W
Reference Clock Frequency 101,0 MHz	CPU Core Temperature 1 36 °C	CPU Core Temperature 2 36 °C	CPU Core Temperature 3 36 °C	CPU Core Temperature 4 36 °C
Memory Frequency 1617 MHz				

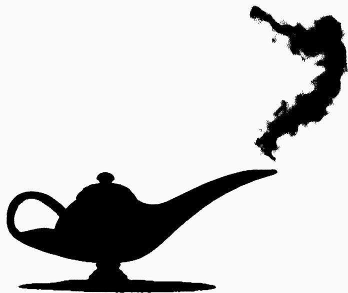
ComputerBase


Intel® Extreme Tuning Utility
Before
Stress Test
Benchmarking
Profiles
App-Profile Pairing
Run XTU Benchmark
How is my system benchmarked?
Current Score
XTU: 1921 Marks
Maximum Processor Frequency 4.15 GHz
Highest CPU Temperature 96 °C
Package Temperature 65 °C
CPU Utilization 5 %
4.14 GHz
5 Minutes

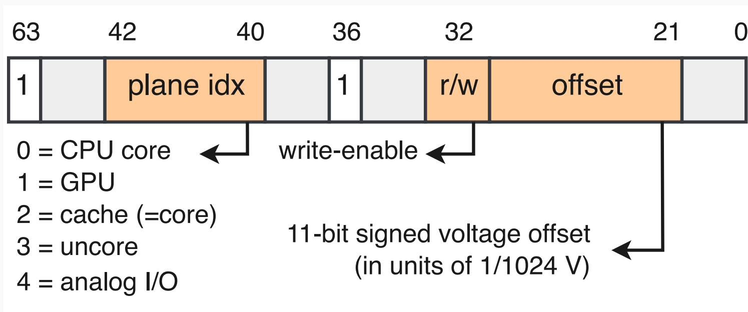
Intel® Extreme Tuning Utility
After
Benchmark your Current Settings
Run XTU Benchmark
How is my system benchmarked?
Current Score
XTU: 2122 Marks
Compare Online
Share, compare, and compete online with other Intel® XTU users in the HWBOT community
Maximum Processor Frequency 4.13 GHz
Highest CPU Temperature 95 °C
Max Core Frequency 4.09 GHz
5 Minutes
I7-9750H
CPU Undervolting
Huge difference!!!

Intel Power Management

Intel Power Management



`msr 0x150`

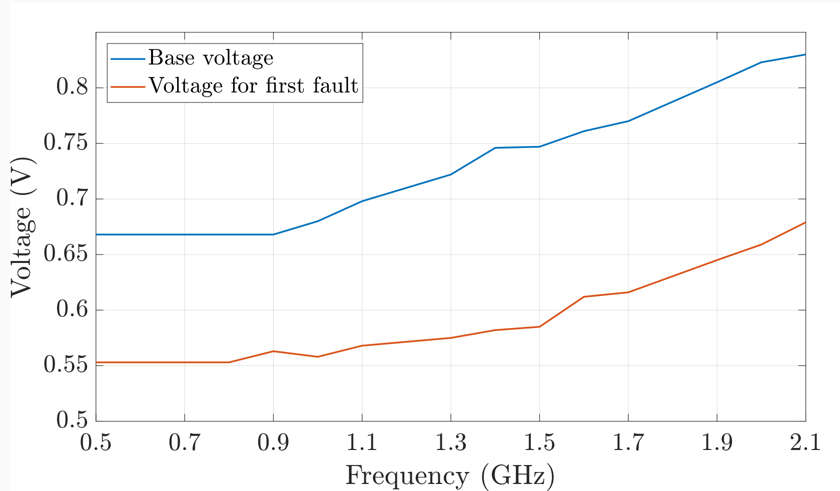

63
42
40
36
32
21
0
1
plane idx
1
r/w
offset
0 = CPU core
1 = GPU
2 = cache (=core)
3 = uncore
4 = analog I/O
write-enable
11-bit signed voltage offset
(in units of 1/1024 V)

Will it fault?

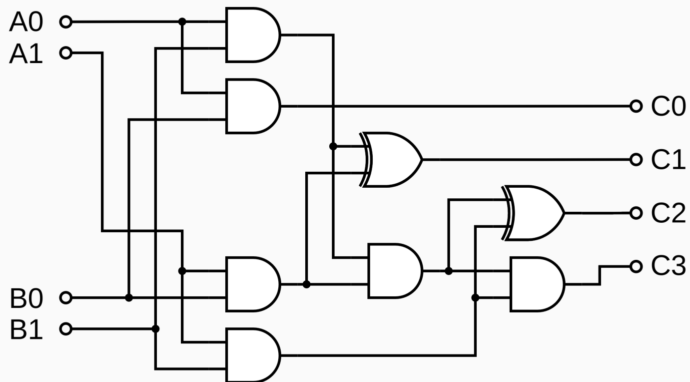
```
uint64_t multiplier = 0x1122334455667788;
uint64_t correct    = 0xdeadbeef * multiplier;
uint64_t var        = 0xdeadbeef * multiplier;

while (var == correct)
{
    var = 0xdeadbeef * multiplier;
}
uint64_t flipped_bits = var ^ correct;
```

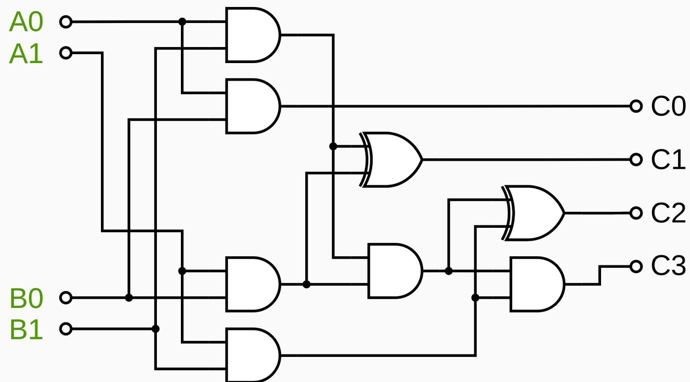
```
bagger>
```

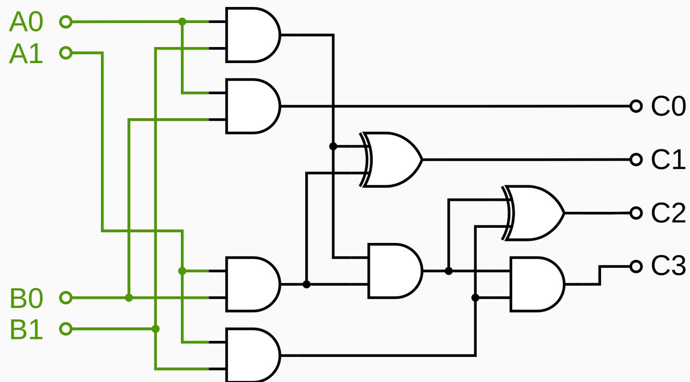
Safe voltages

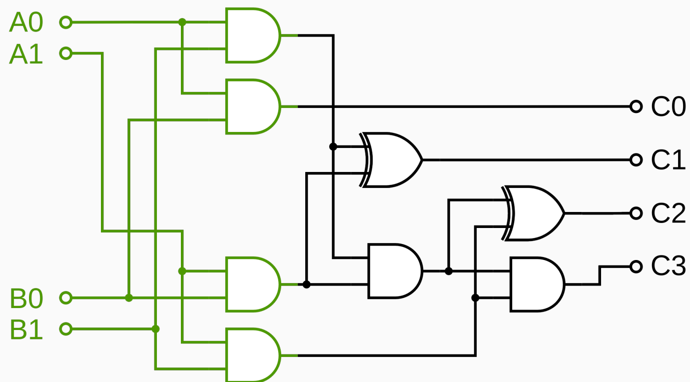


Correct Multiplication




A0
A1
B0
B1
C0
C1
C2
C3


A0
A1
B0
B1
C0
C1
C2
C3


A0
A1
B0
B1
C0
C1
C2
C3

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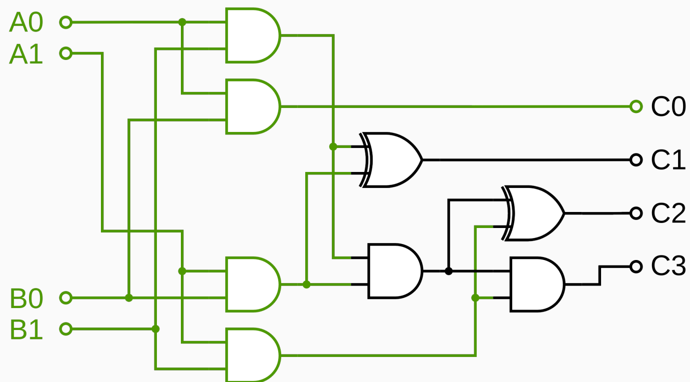

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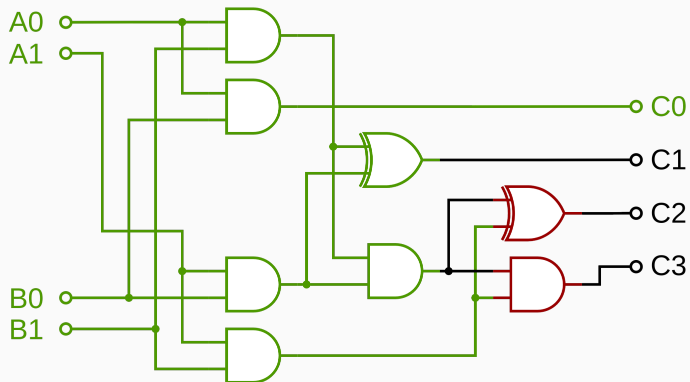

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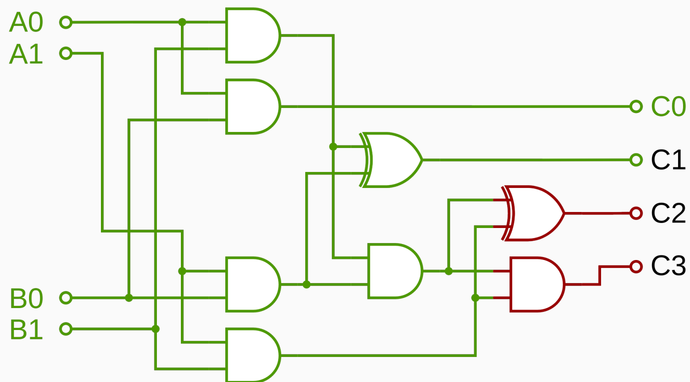
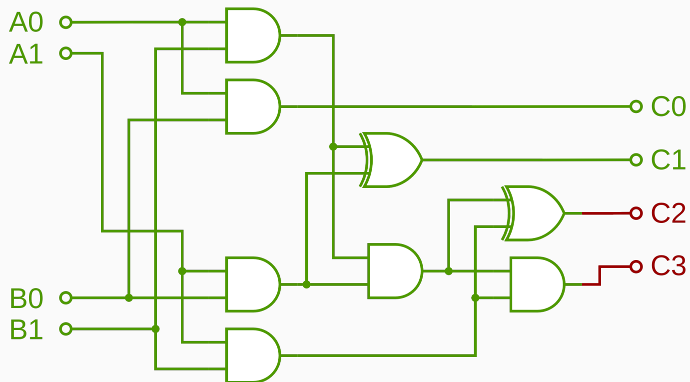
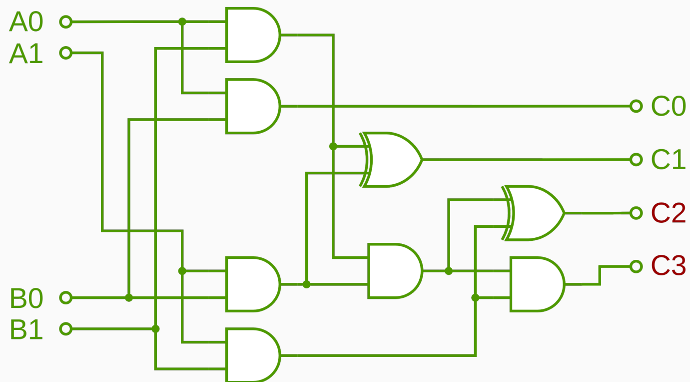
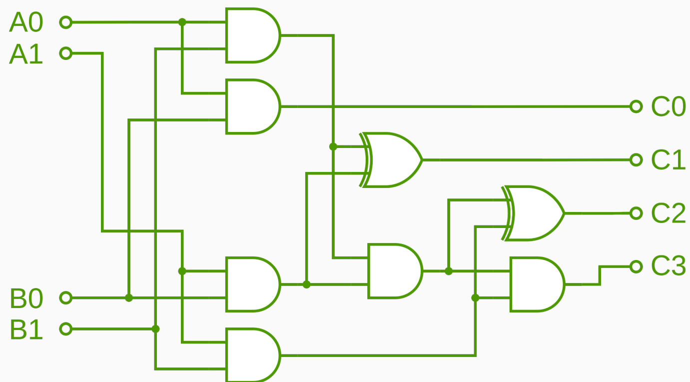
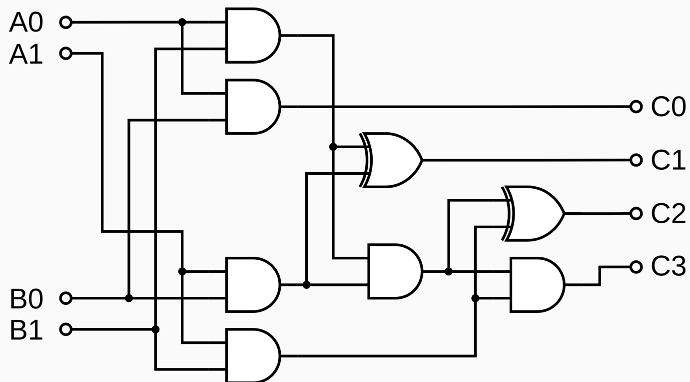
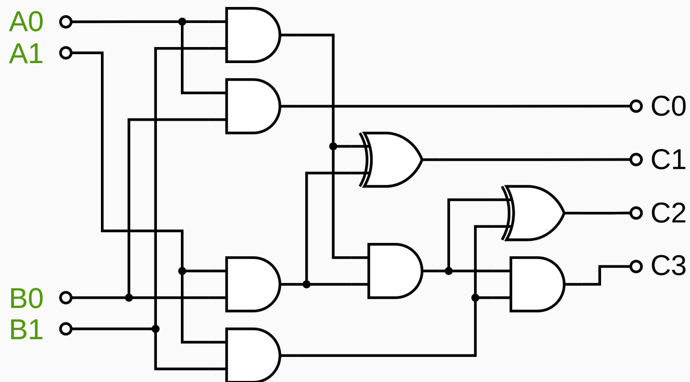


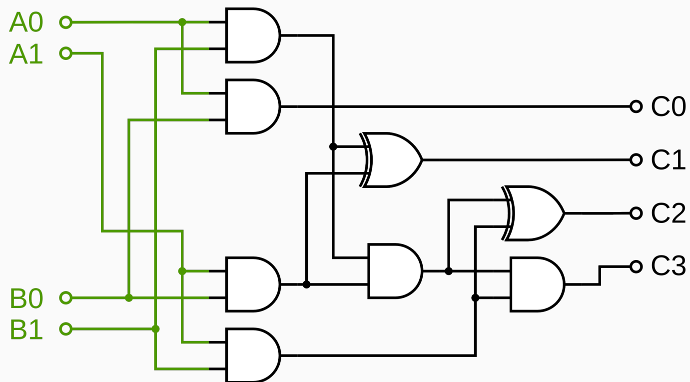

A0
A1
B0
B1
C0
C1
C2
C3

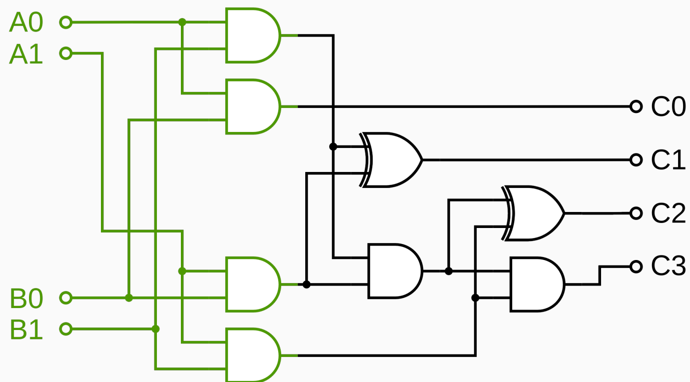

A0
A1
B0
B1
C0
C1
C2
C3

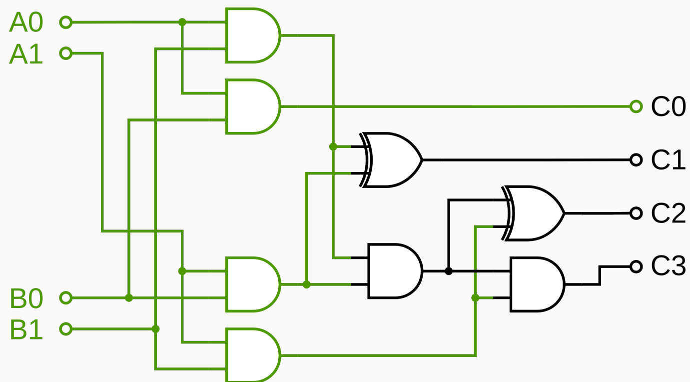

A0
A1
B0
B1
C0
C1
C2
C3


A0
A1
B0
B1
C0
C1
C2
C3


A0
A1
B0
B1
C0
C1
C2
C3


A0
A1
B0
B1
C0
C1
C2
C3


A0
A1
B0
B1
C0
C1
C2
C3


A0
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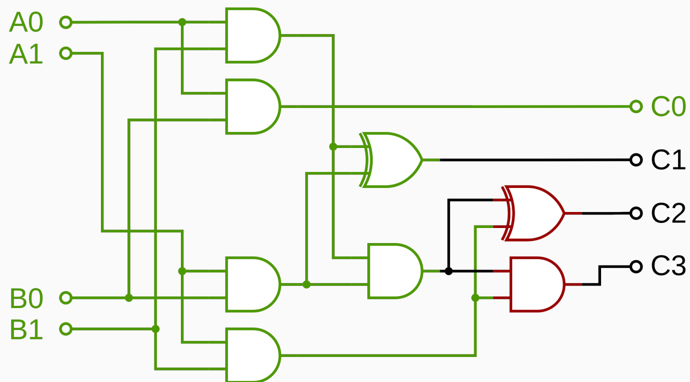
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A1
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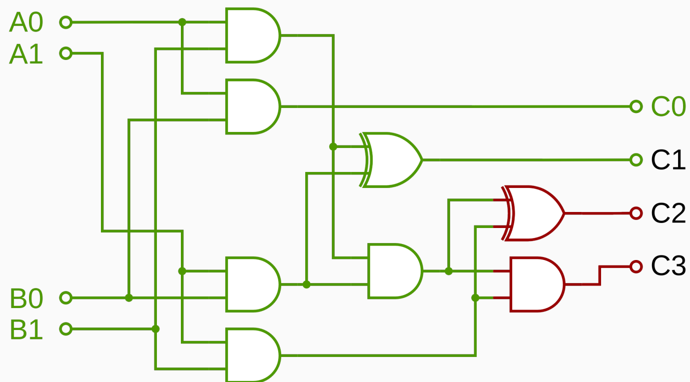
C3


A0
A1
B0
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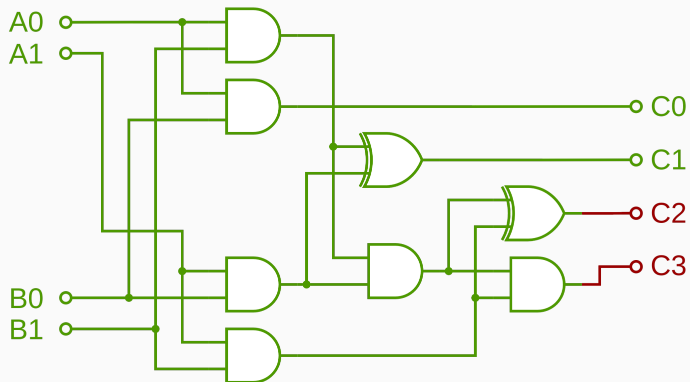
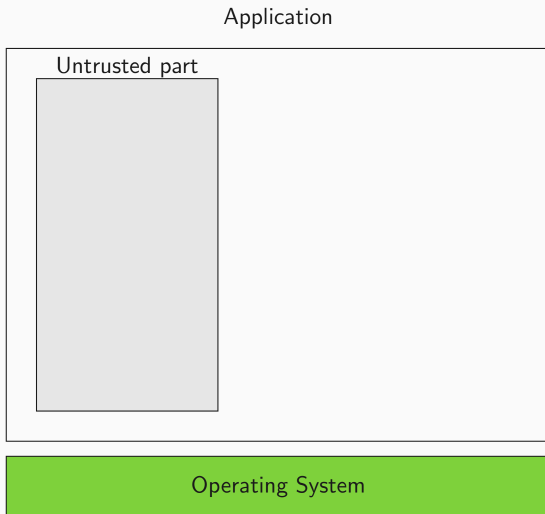
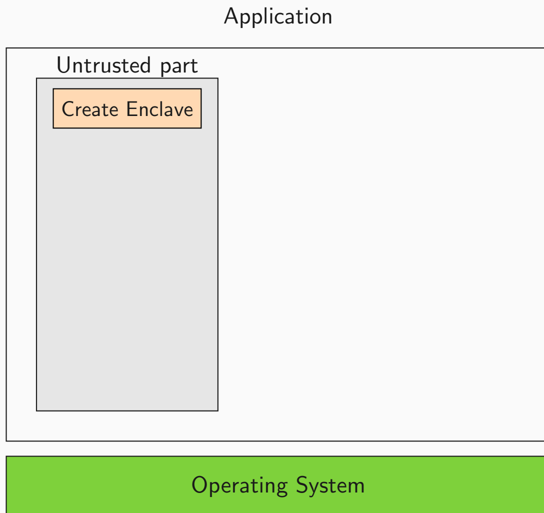
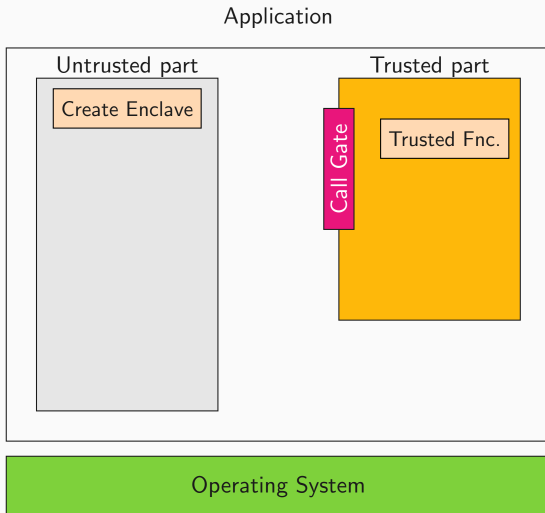
C0
C1
C2
C3

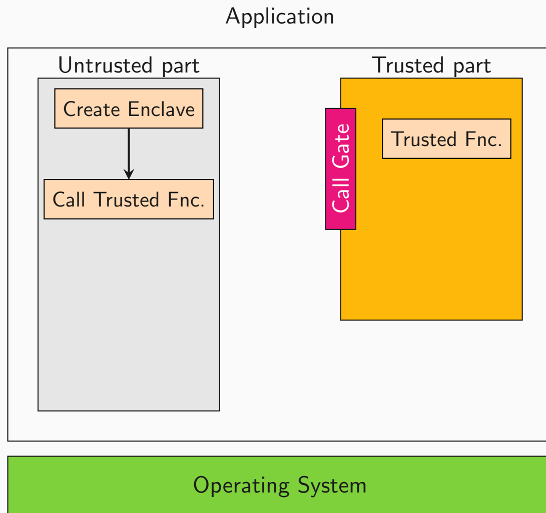
Faulty Multiplication

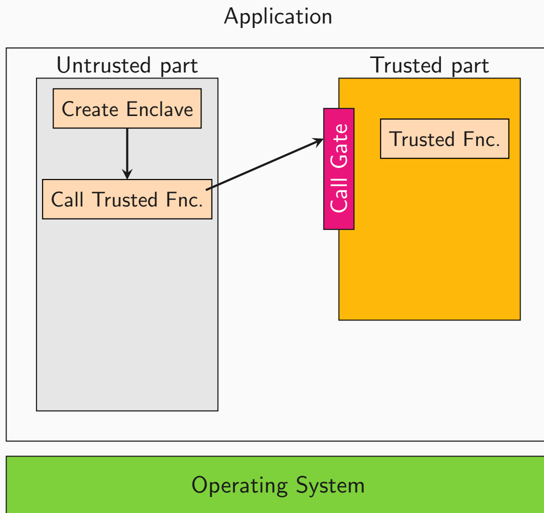



Application
Untrusted part
Operating System


Application
Untrusted part
Create Enclave
Operating System


Application
Untrusted part
Create Enclave
Trusted part
Call Gate
Trusted Fnc.
Operating System


Application
Untrusted part
Create Enclave
Call Trusted Fnc.
Trusted part
Call Gate
Trusted Fnc.
Operating System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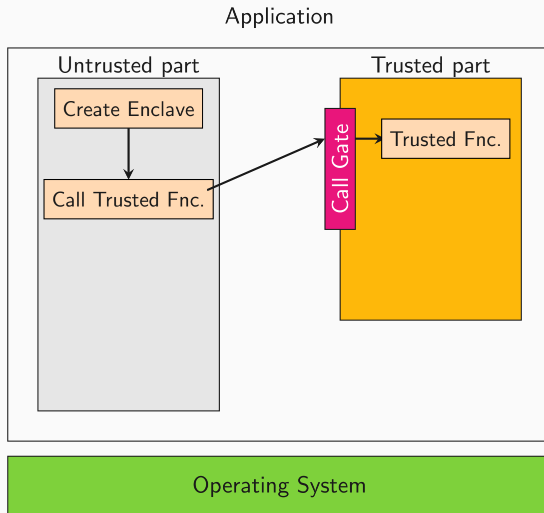
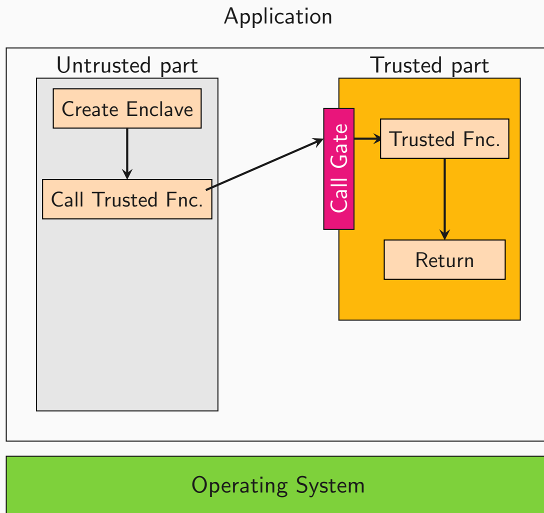
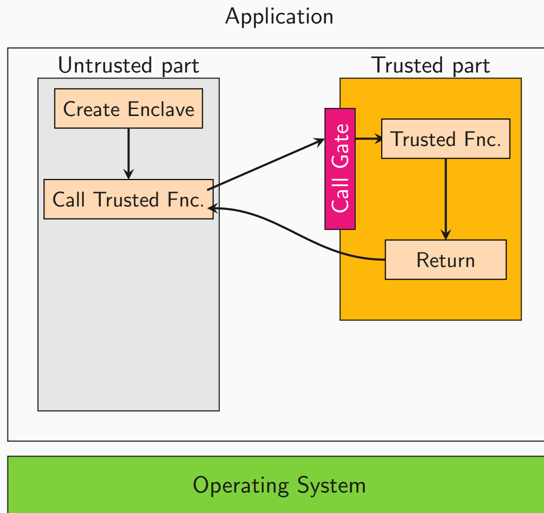
Trusted part
Create Enclave
Call Trusted Fnc.
Call Gate
Trusted Fnc.
Operating System


Application
Untrusted part
Trusted part
Create Enclave
Call Trusted Fnc.
Call Gate
Trusted Fnc.
Operating System


Application
Untrusted part
Trusted part
Create Enclave
Call Trusted Fnc.
Call Gate
Trusted Fnc.
Return
Operating System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Create Enclave
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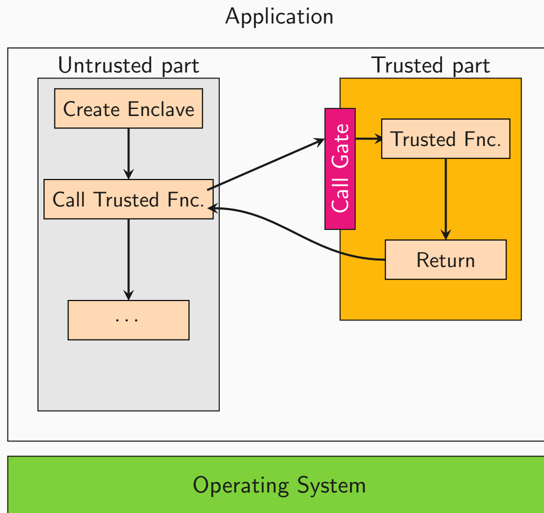
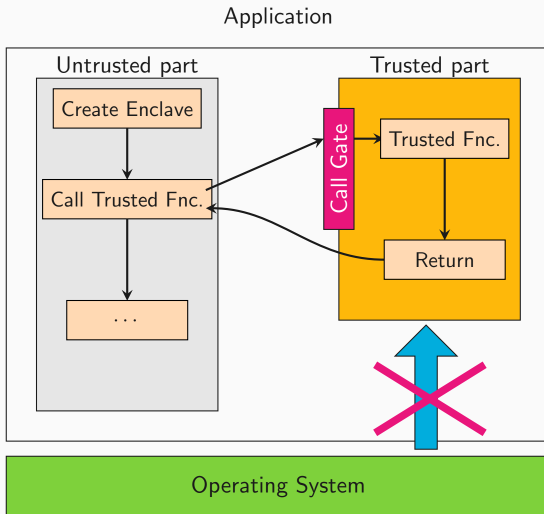
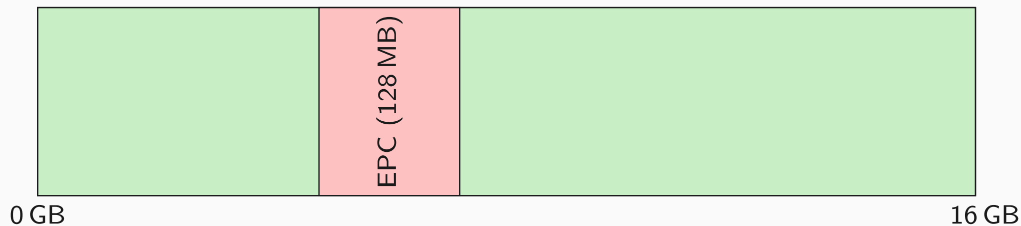
Trusted Fnc.
Return
Operating System


Application
Untrusted part
Trusted part
Create Enclave
Call Trusted Fnc.
...
Call Gate
Trusted Fnc.
Return
Operating System

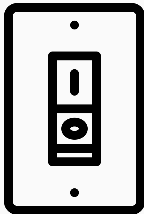

Application
Untrusted part
Trusted part
Create Enclave
Call Trusted Fnc.
...
Call Gate
Trusted Fnc.
Return
Operating System

0 GB
16 GB

SGX Encrypted Memory

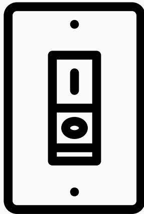


Bit Flips in the EPC

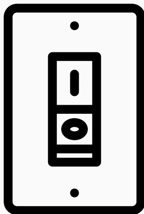


- Bit flips in the EPC?

Bit Flips in the EPC

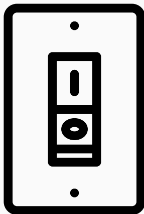


- Bit flips in the EPC?
- Integrity check fails!



- Bit flips in the EPC?
- Integrity check fails!

→ Lock up memory controller



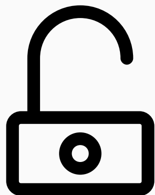
- Bit flips in the EPC?
- Integrity check fails!

→ Lock up memory controller

→ System halts immediately (no exploit, but DoS!)

Will SGX save us?

```
                                              [Userspace] Voltage: -261 mV
[Enclave] Multiplying 0xdeadbeef 0x1122334455667788
[Enclave] Multiply_it. result: 0.
```



- Public Key Crypto
- Encrypt/Sign messages
- Untrusted channel
- Encrypt/Verify messages with public key
- Decrypt/Sign messages with private key

RSA Signature with Chinese Remainder Theorem

$$n = \mathrm{p} \times q$$

$$S = H^{d} \bmod n$$

RSA Signature with Chinese Remainder Theorem

$$n = p \times q$$

$$S = H^{d} \bmod n$$

$$d_p = d \bmod p - 1$$

$$d_q = d \bmod q - 1$$

$$s_1 = H^{d_p} \bmod p$$

$$s_2 = H^{d_q} \bmod q$$

$$n = \mathrm{p} \times q$$

$$S = ((q^{-1} \bmod p)(s_1 - s_2) \bmod p) \times q + s_2$$

$$d_p = d \bmod p - 1$$

$$d_q = d \bmod q - 1$$

$$s_1 = H^{d_p} \mod p$$

$$s_2 = H^{d_q} \mod q$$

$$n = \mathrm{p} \times q$$

$$S = ((q^{-1} \bmod p)(s_1 - s_2) \bmod p) \times q + s_2$$

$$d_p = d \bmod p - 1$$

$$d_q = d \bmod q - 1$$

$$s_1 = H^{d_p} \bmod p$$

$$s_2 = H^{d_q} \bmod q$$

$$n = \mathrm{p} \times q$$

$$S = ((q^{-1} \bmod p)(s_1 - s_2) \bmod p) \times q + s_2$$

$$S' = ((q^{-1} \bmod p)(s_1 - s_2) \bmod p) \times q + s_2$$

$$n = p \times q$$

$$S = (\text{something}) \times q + s_2$$

$$S' = (\text{something else}) \times q + s_2$$

RSA Signature with Chinese Remainder Theorem

$$n = p \times q$$

$$S = (\text{something}) \times q + s_2$$

$$S' = (\text{something else}) \times q + s_2$$

$$S - S' = \text{something} \times q$$

$$n = p \times q$$

$$S = (\text{something}) \times q + s_2$$

$$S' = (\text{something else}) \times q + s_2$$

$$S - S' = \text{something} \times q$$

$$q = \gcd(S - S', n)$$

RSA decryption

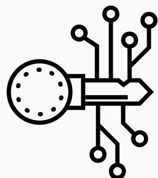

```c
uint8_t rsa_dec_ecall(int iterations)
{
    // Wait for first fault
    trigger_fault(iterations);

    // Actual decryption
    ippsRSA_Decrypt(ct, dec, pPrv, scratchBuffer);
}
```

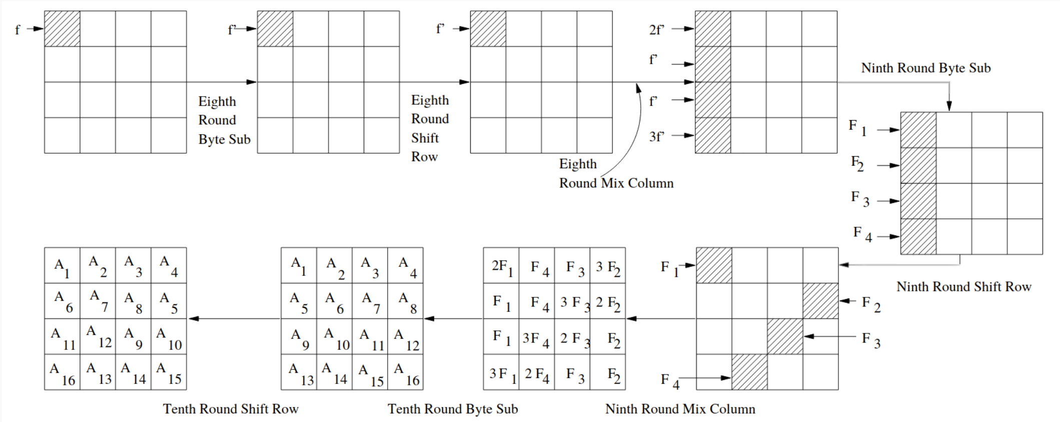
```
bagger> dog Enclave/encl
```

WHAT ELSE CAN WE BREAK?!

AES Basics



- Symmetric Key Crypto
- Encrypt messages for transfer over public channel
- Encrypt data for (untrusted) storage
- 4×4 byte state
- 10 rounds: S-Box, ShiftRows, MixColumns, AddRoundKey



Tunstall2011

AES-NI (New Instructions)

Instruction	Description
`AESENC`	Perform one round of an AES encryption flow
`AESENCLAST`	Perform the last round of an AES encryption flow
`AESDEC`	Perform one round of an AES decryption flow
`AESDECLAST`	Perform the last round of an AES decryption flow
`AESKEYGENASSIST`	Assist in AES round key generation
`AESIMC`	Assist in AES Inverse Mix Columns
`PCLMULQDQ`	Carryless multiply (CLMUL)

AES New Instructions - inside SGX


```
do
{
        i++;
        plaintext = <randomly generated>

        result1 = aes128_enc(plaintext);
        result2 = aes128_enc(plaintext);
} while (vec_equal_128(result1,result2) && i<iterations);
```

```
bagger> sudo ./aes-encrypt 100000 -262
```

THIS IS MORE THAN JUST CRYPTO

But what about memory corruption?


```
struct_foo_t *foo = &arr[offset];
foo->foo = enclave_secret;
```

But what about memory corruption?

```
struct_foo_t *foo = &arr[offset];
foo->foo = enclave_secret;
```

But what about memory corruption?

```
foo = arr + offset * 0x24
```

But what about memory corruption?

```
foo = arr + offset * 0x24
```

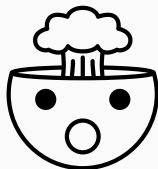
```
Creating enclave...
==== Victim Enclave ====
[pt.c] /dev/sgx-step opened!
Enclave Base:    0x7f001a000000
Enclave Limit:   0x7f001c000000
EDBGRD: debug
```

Voltage
0.584V

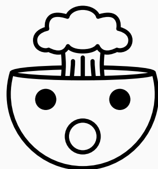
Undervolting
-235mV

More than just crypto?

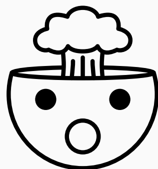
More than just crypto?



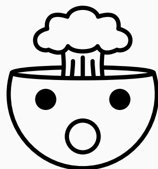
More than just crypto?



More than just crypto?

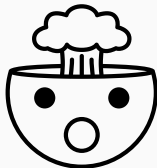


- RSA keys

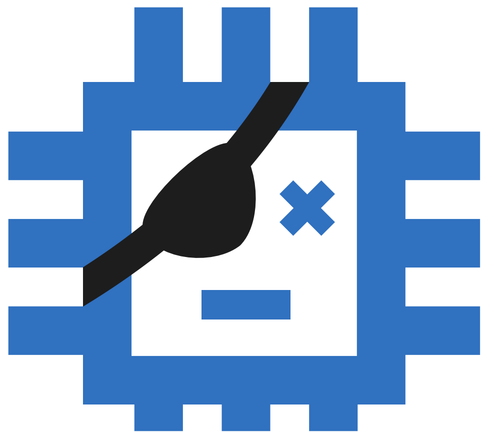


- RSA keys
- AES keys

More than just crypto?



- RSA keys
- AES keys
- Memory corruption



PLUNDER
VOLT

- A new type of attack

Plundervolt TLDR

- A new type of attack
- Breaks the integrity of SGX

Plundervolt TLDR

- A new type of attack
- Breaks the integrity of SGX
- Within SGX we:

- A new type of attack
- Breaks the integrity of SGX
- Within SGX we:
  - Retrieve keys from AES-NI

Plundervolt TLDR

- A new type of attack
- Breaks the integrity of SGX
- Within SGX we:
    - Retrieve keys from AES-NI
    - Retrieve RSA signature key

Plundervolt TLDR

- A new type of attack
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- Within SGX we:
  - Retrieve keys from AES-NI
  - Retrieve RSA signature key
  - Induce memory corruption in bug free code

Plundervolt TLDR

- A new type of attack
- Breaks the integrity of SGX
- Within SGX we:
  - Retrieve keys from AES-NI
  - Retrieve RSA signature key
  - Induce memory corruption in bug free code
  - Make enclave write secrets to untrusted memory

Side-Channel Security

Chapter 6: Software-based Fault Attacks

Jonas Juffinger

April 11, 2024

www.iaik.tugraz.at

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