Side-Channel Security

Chapter 3: Trusted Execution Environments

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Trusted Execution Environments (TEEs)

Motivation

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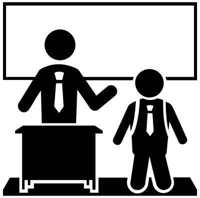
- Providers: tamper-resistant way
- Protect computation against compromised OS
- Key enabler of trusted cloud computing

Intel Software Guard Extension (SGX)

SGX Introduction



- x86 instruction-set extension

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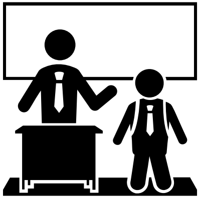

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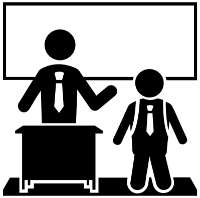

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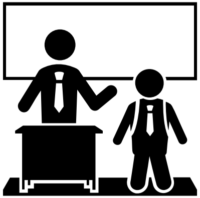

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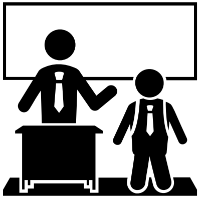

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- Enclave full access to virtual memory of host application

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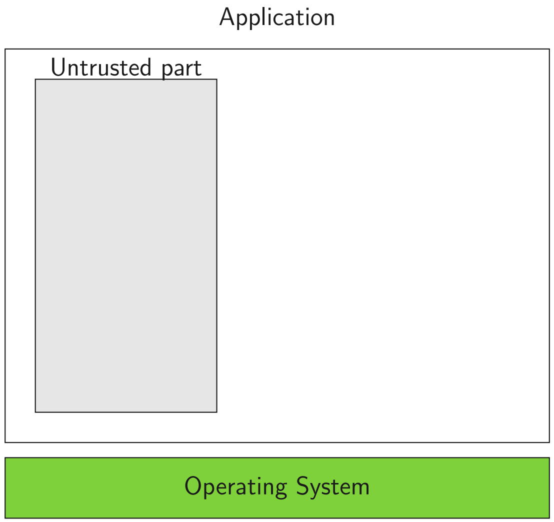

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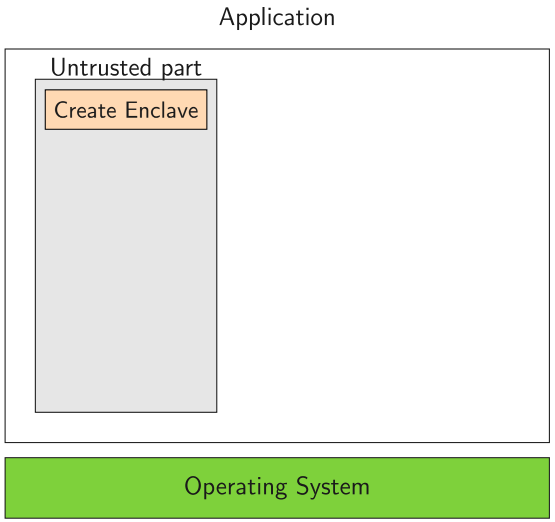
Application
Untrusted part
Create Enclave
Operating System

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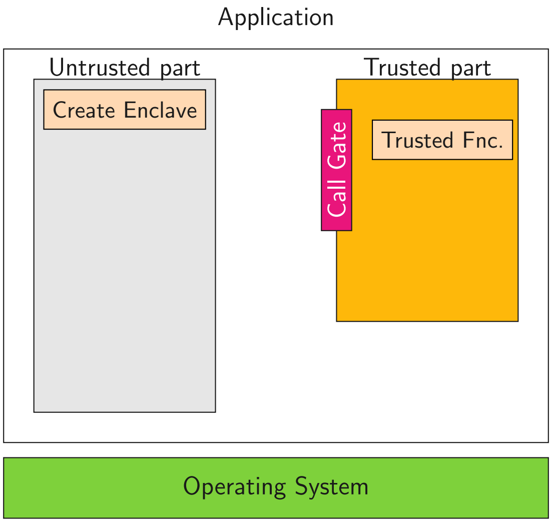
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Trusted Fnc.
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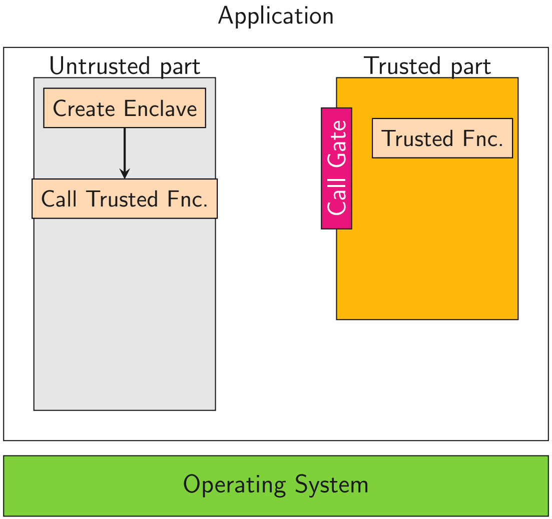
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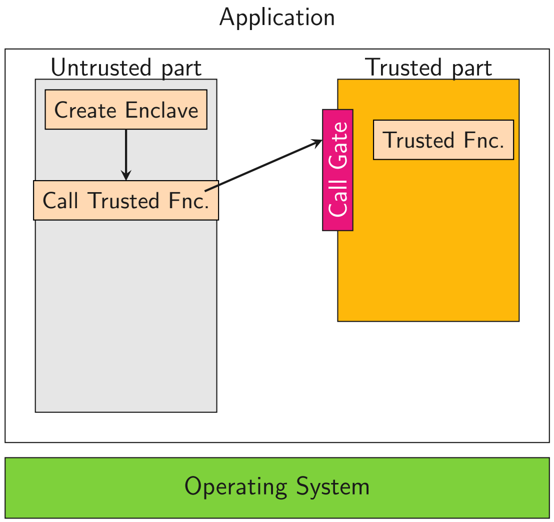
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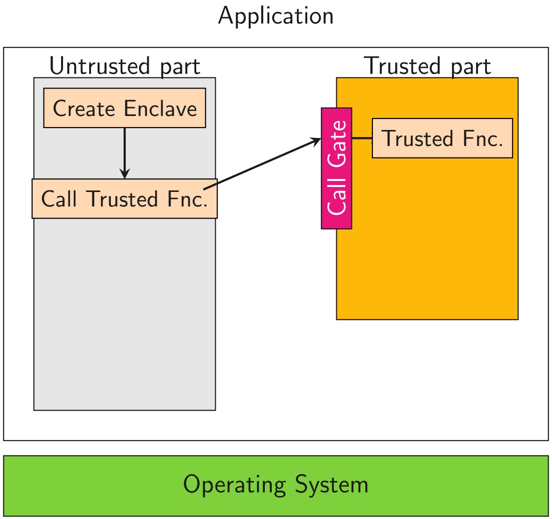
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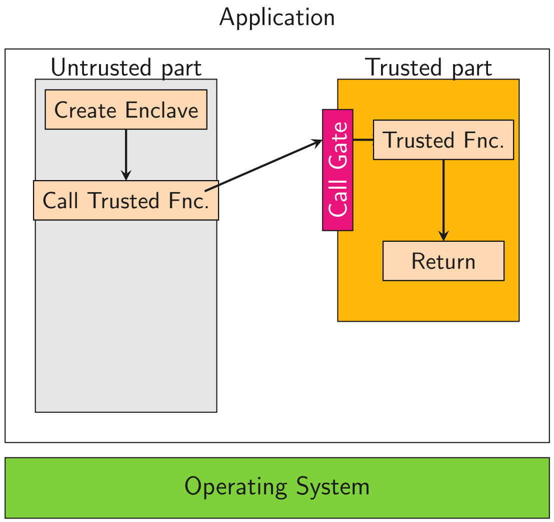
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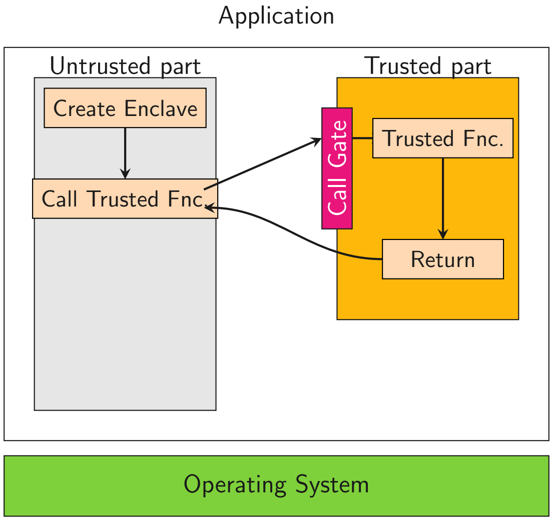
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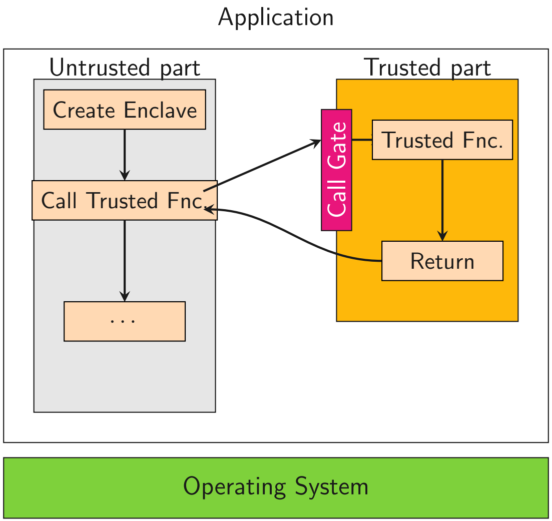
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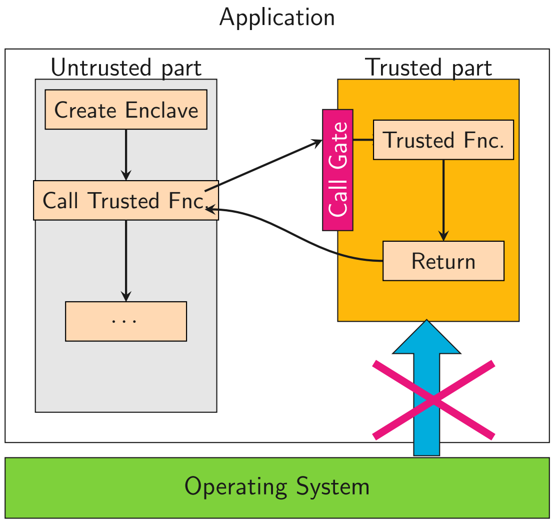

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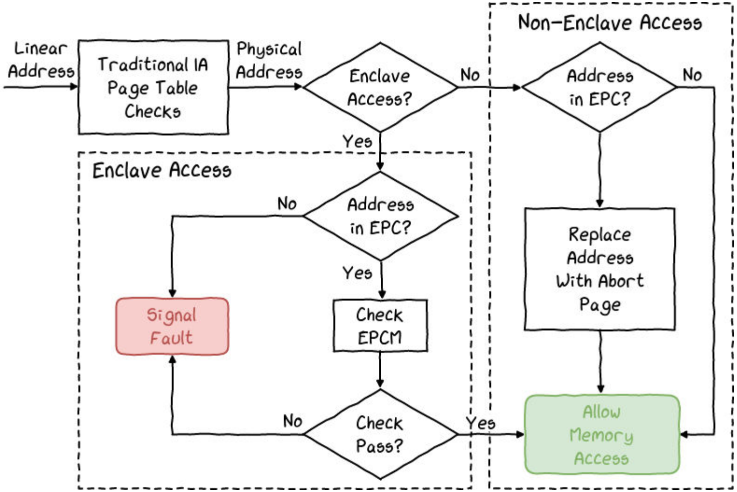
Address Translation



Restrictions

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- Certain instructions are forbidden (e.g., *rdtsc*)

Interrupt and Resume Enclave

1. Interrupt arrives

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5. *ERESUME*

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- Allows physical attacker
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- Side-Channel Attacks are out of scope
- Only CPU is trusted

Attack Targets

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Side-Channel Attacks:

Page Table

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DRAM

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Side-Channel Attacks:

Page Table

DRAM

Cache

Attack Targets

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Predictors

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Interrupt

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Transient-Execution Attacks (Lecture 3):

Attack Targets

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Page Table

DRAM

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Transient-Execution Attacks (Lecture 3):

Meltdown

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Fault Attacks (Lecture 5):

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Page Table

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Page Table

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Fault Attacks (Lecture 5):

Controlled-Channel Attacks [8]

- Target mechanism which translates virtual to physical addresses

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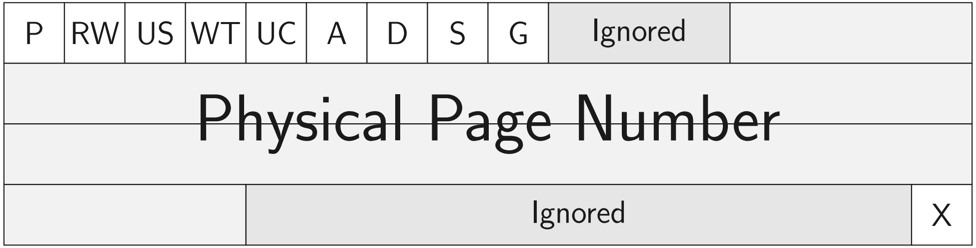
- Consequence: OS can unmap page, observe page fault
- Granularity: 1 page (4kB)

Stealthier Controlled-Channel Attacks [6, 7]



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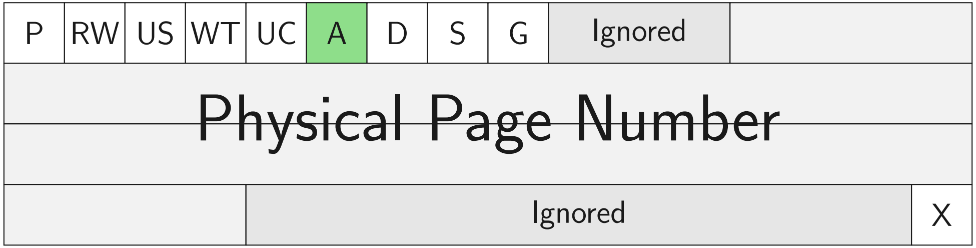

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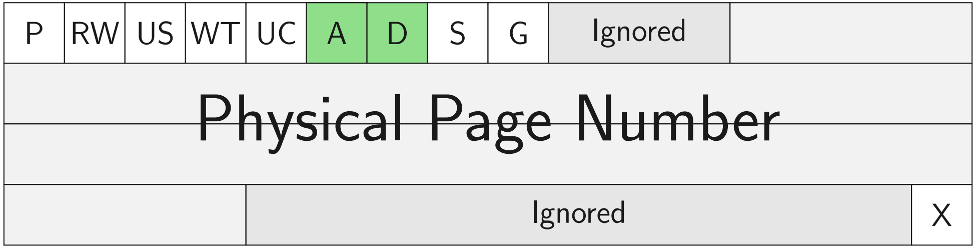

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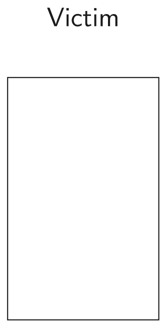
- Examples: [5], [7], [1], [3]

Malware Guard Extension [5]



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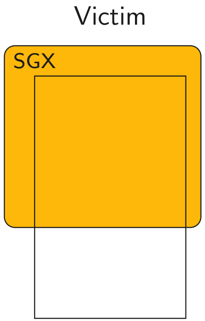

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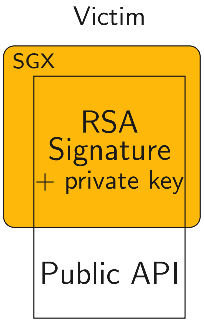

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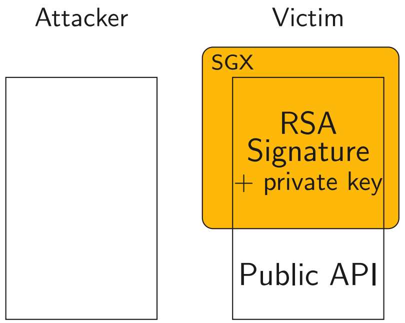

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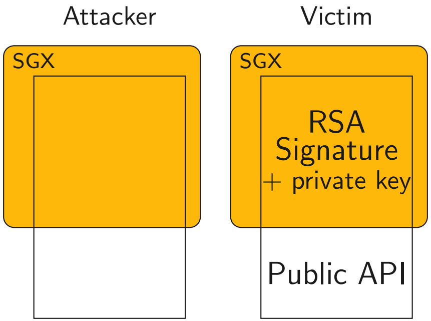

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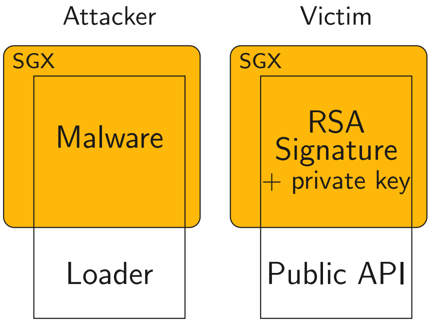

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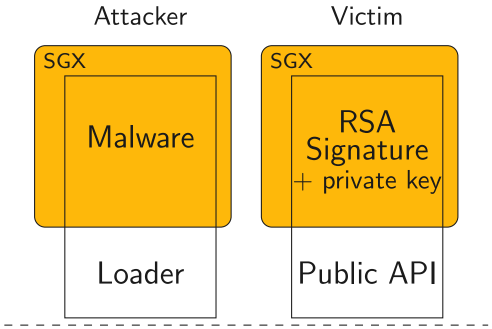

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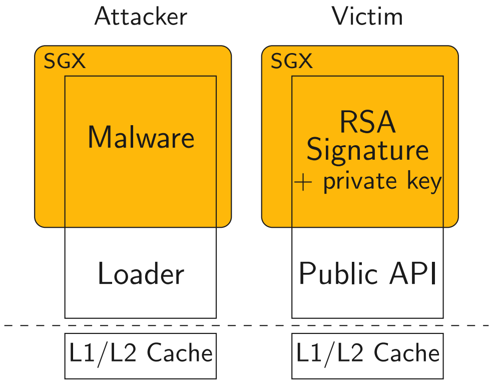

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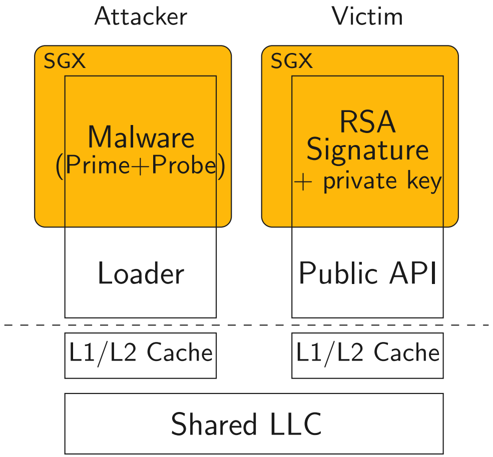

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- No syscalls
- No shared memory
- No physical addresses
- No 2 MB large pages

Timer

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- Start a thread that continuously increments a global variable

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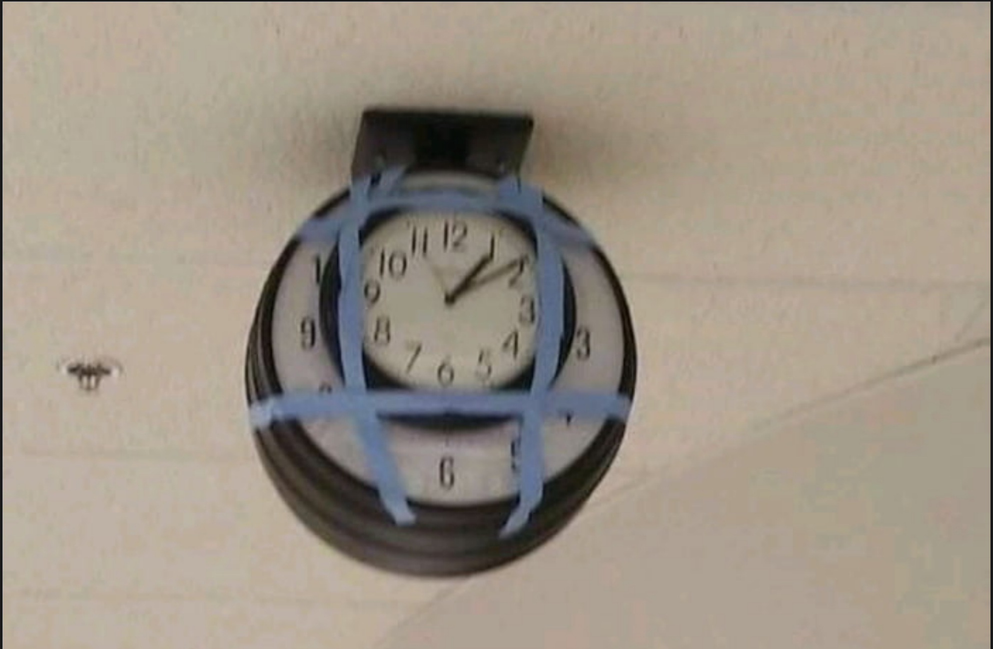
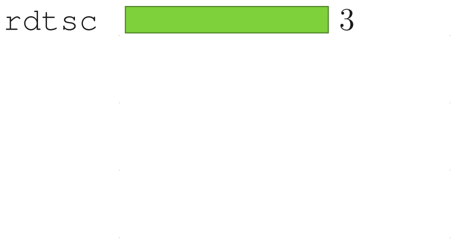
- Start a thread that continuously increments a global variable
- The global variable is our timestamp



ARE YOU REALLY EXPECTING TO
OUTPERFORM THE HARDWARE COUNTER?

Self-built Timer

CPU cycles one increment takes



```
timestamp = rdtsc();
```

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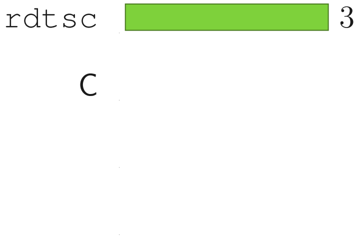

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while(1) {
  timestamp++;
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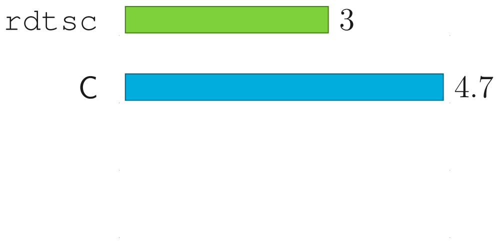

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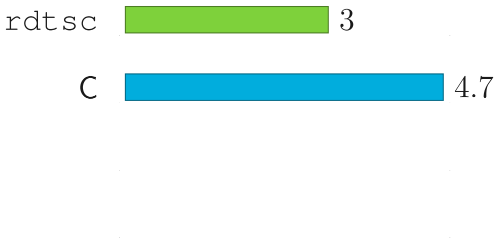

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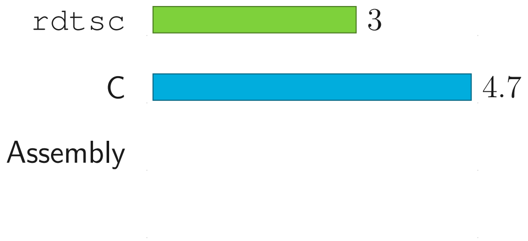

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mov &timestamp, %rcx
  1: incl (%rcx)
  jmp 1b
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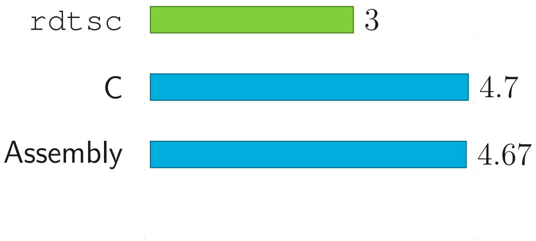

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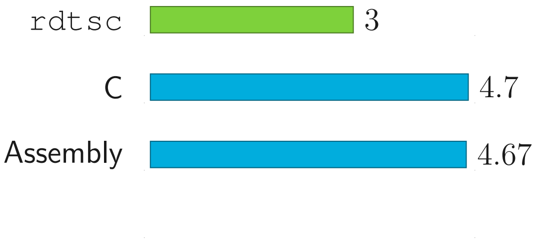

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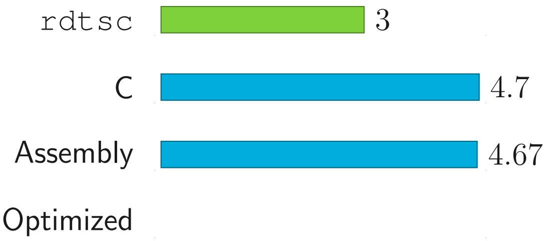

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1: inc %rax
mov %rax, (%rcx)
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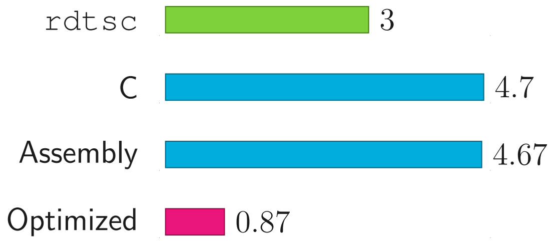

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Combining Everything

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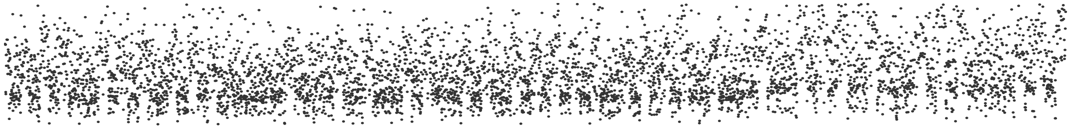
3. Mount Prime+Probe on the buffer containing the multiplier

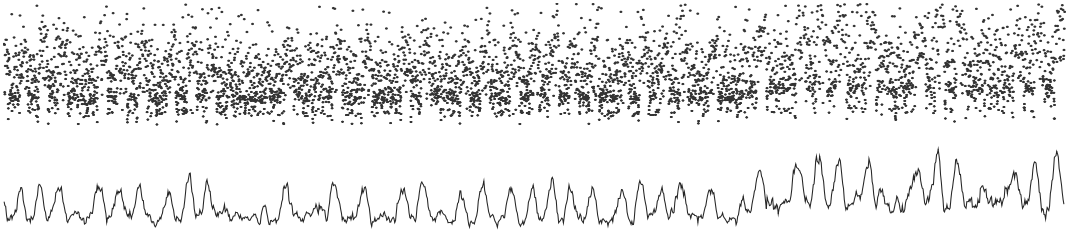
Measured Trace

Raw Prime+Probe trace...



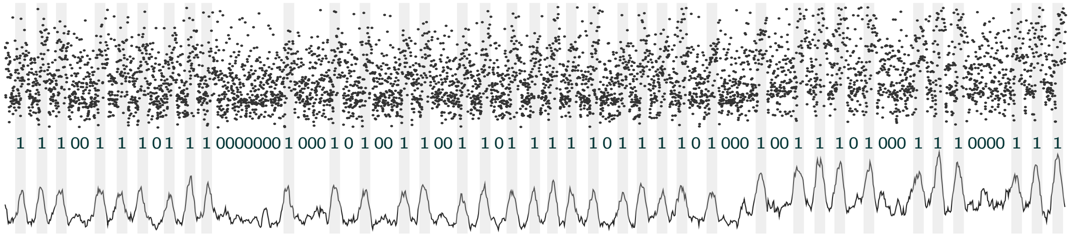
Measured Trace

...processed with a simple moving average...



Measured Trace

...allows to clearly see the bits of the exponent



Single-Stepping

- local Advanced Programmable Interrupt Controller (APIC)

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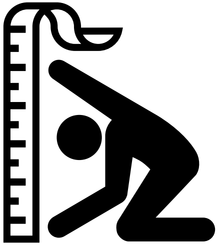

- local Advanced Programmable Interrupt Controller (APIC)
- Timer: 3 modes

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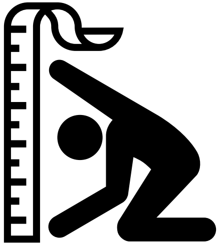

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  - One-shot

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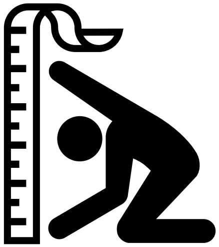

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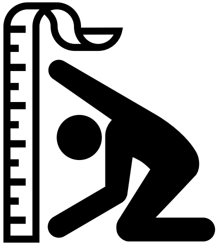
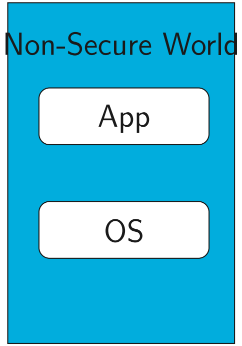
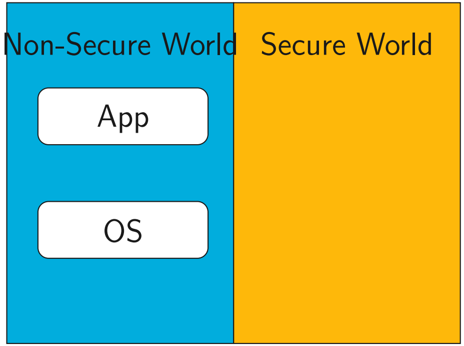


- local Advanced Programmable Interrupt Controller (APIC)
- Timer: 3 modes
    - One-shot
    - Periodic
    - TSC-deadline

ARM TrustZone



ARM TrustZone



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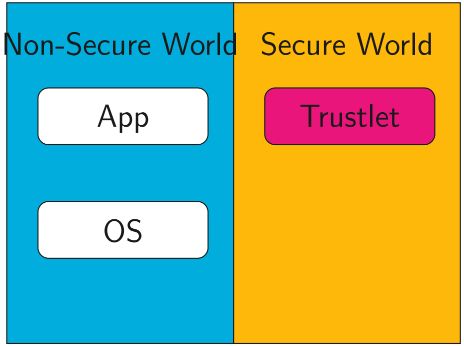

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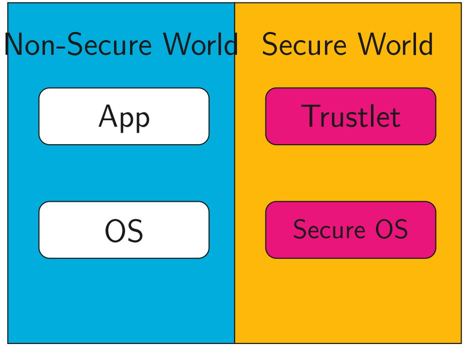

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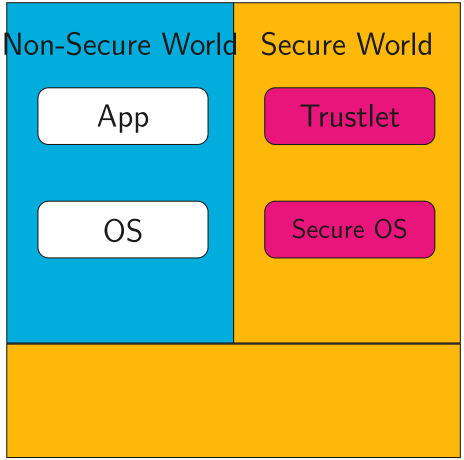

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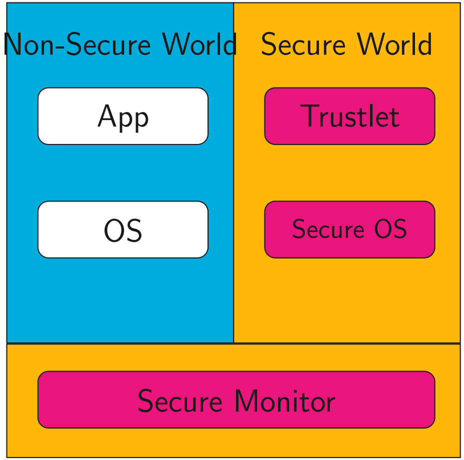

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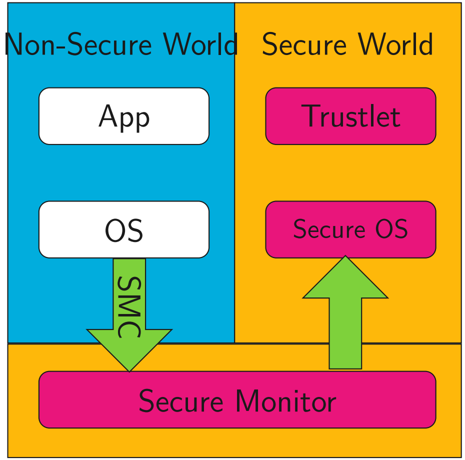
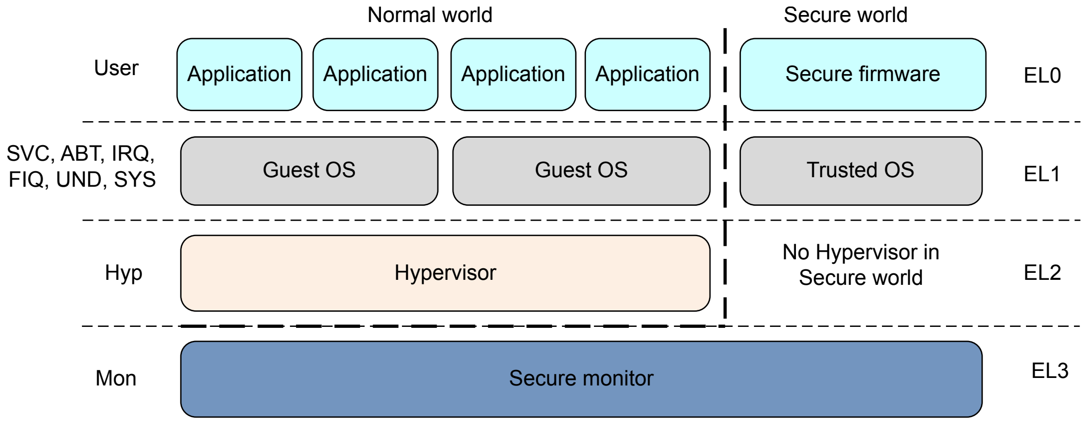
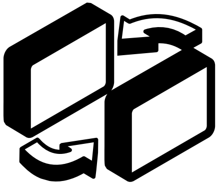


Exception Levels

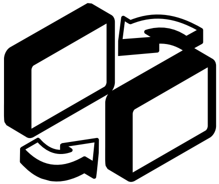


Switching Worlds



- 2 Virtual Processors: time-sliced fashion operation

Switching Worlds



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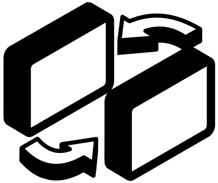

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Switching Worlds

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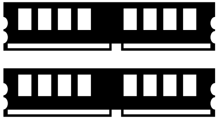
- Peripherals: interrupt controllers, timers, user I/O devices (APB)

Attack 1: Double Fetches [4]



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Attack 1: Double Fetches [4]

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- Caused by accessing the shared memory twice
- Also called double-fetch bugs

A Double Fetch

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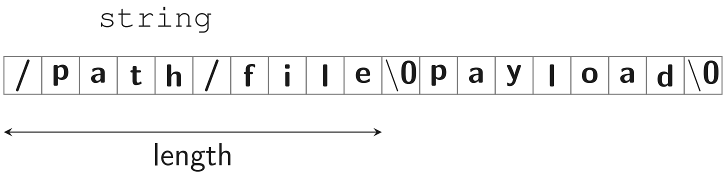

Thread 1

Thread 2

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strcpy(string, "/path/file\0
    payload");
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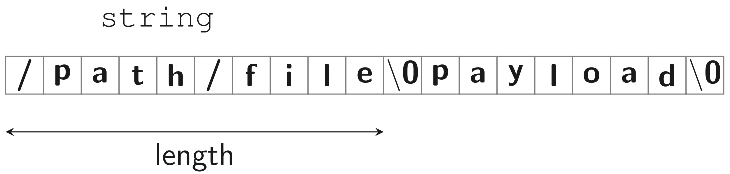

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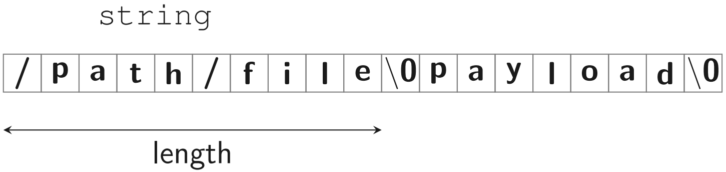

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char* local = malloc(len + 1);
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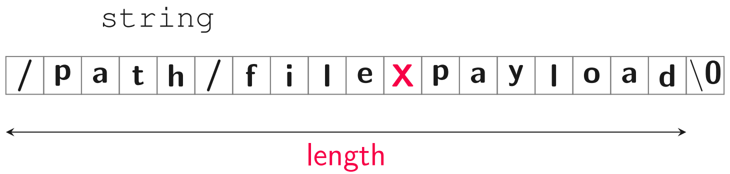

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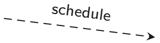

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string[10] = 'X';
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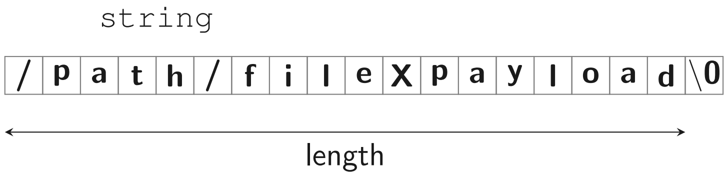

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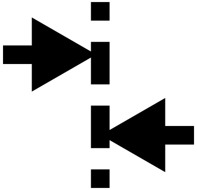

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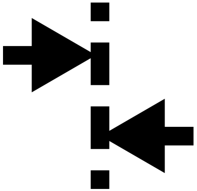
Double Fetches



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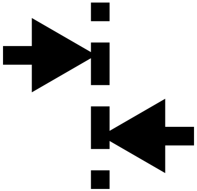

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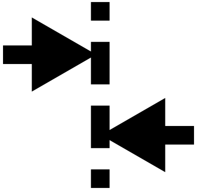

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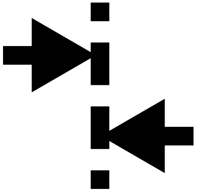

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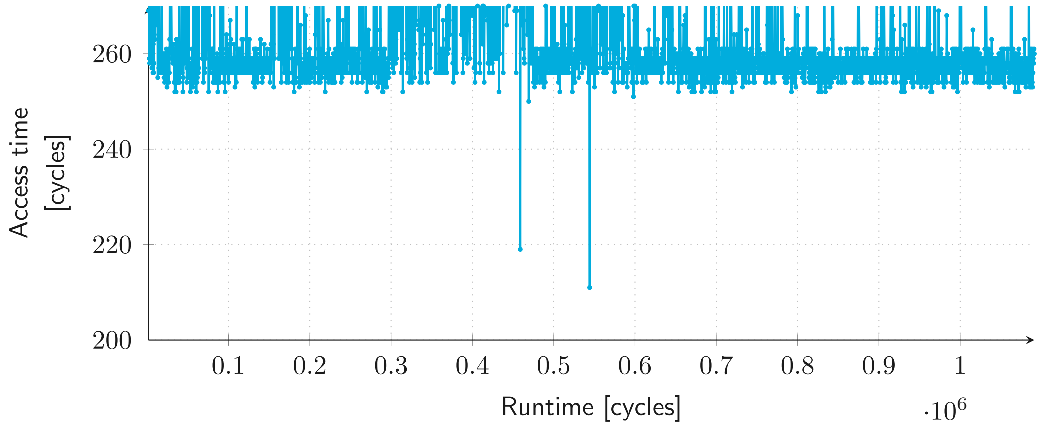
- Changing data after sanity check allows exploitation
- Critical if privilege boundaries are crossed
  - User space ↔ Kernel space
  - Untrusted code ↔ Trusted code
- Common to share data across these domains

Double-fetch Detection



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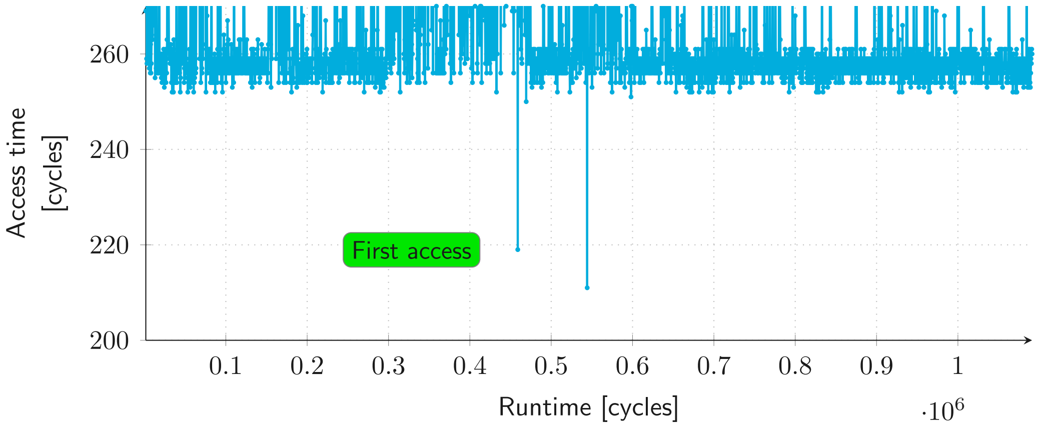

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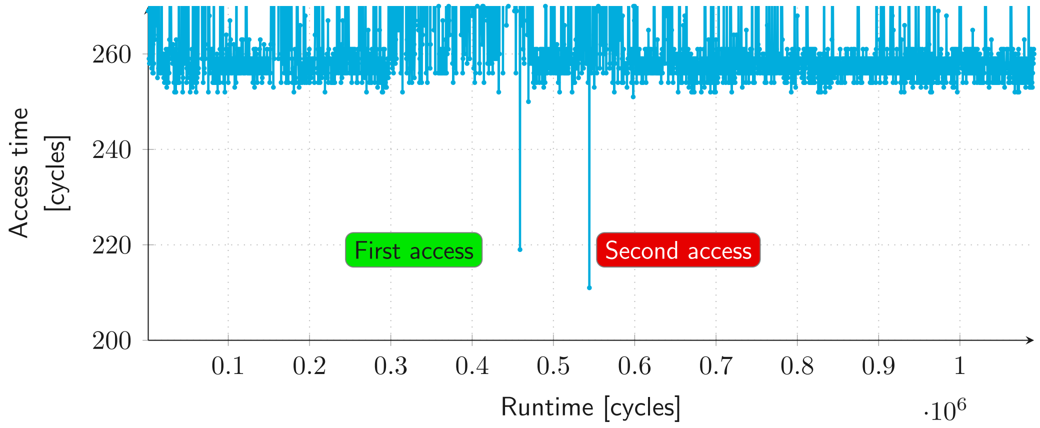

Attack 2: Armageddon [2]

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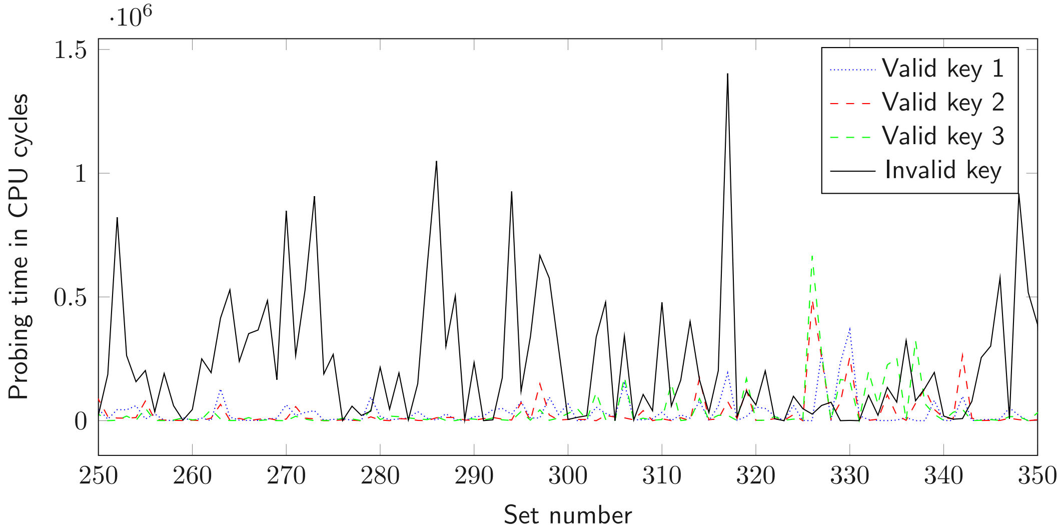
  - Secure element for payments
  - DRM
- TrustZone leaks through the cache

Leakage from ARM TrustZone (RSA signatures)



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Side-Channel Security

Chapter 3: Trusted Execution Environments

Daniel Gruss

March 14, 2024

Graz University of Technology

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