# Operating Systems

## Virtual Memory Basics

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# Address Translation

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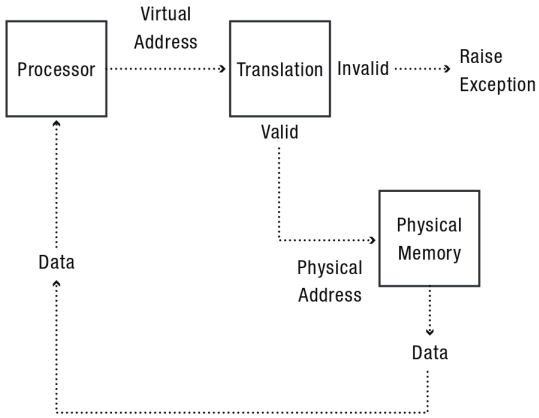
- programmers perspective:
  - pointers point to objects etc.
  - transparent: it is not necessary to know how memory reference is converted to data

# Address Translation - Idea / Overview



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  - Multiple regions for dynamic allocation (heaps/stacks)

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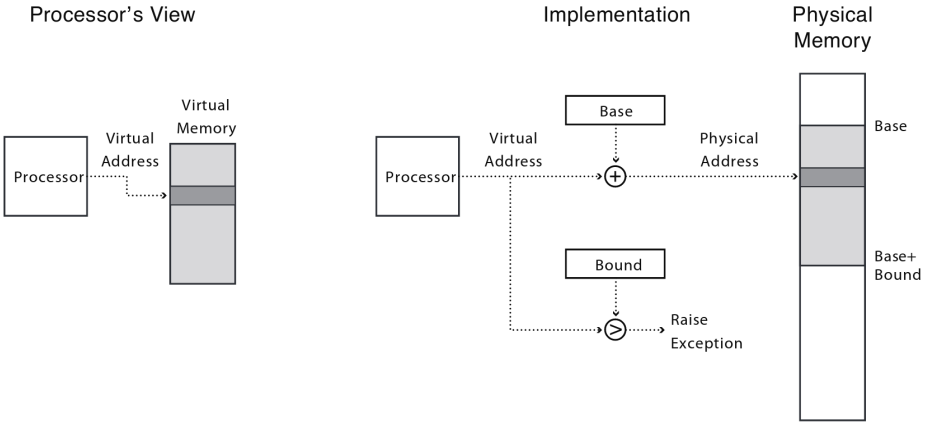
# Base-Limit or Base and bounds



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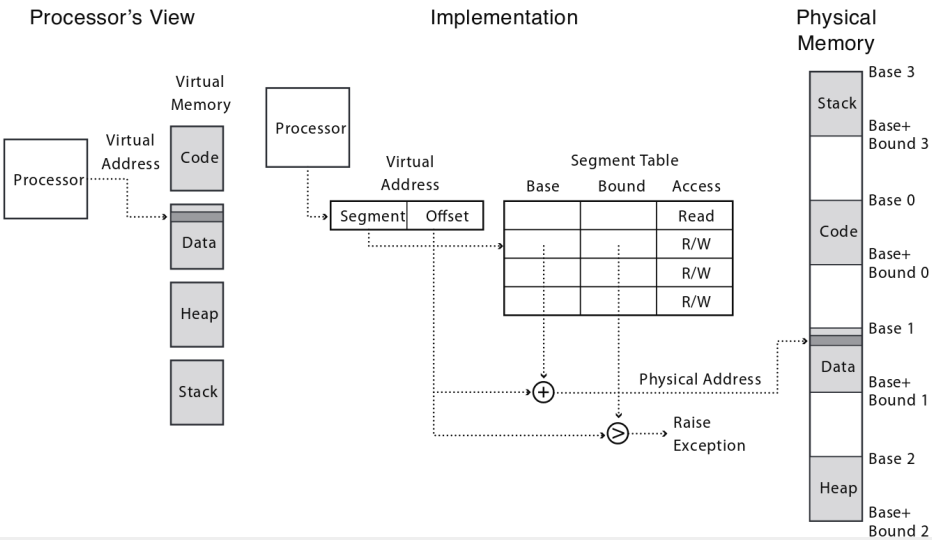

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  - Each segment has: start, length, access permission

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  - correct programs will not generate references outside valid memory
  - trying to read or write data that does not exist: bug-indication

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$\rightarrow$ set segment read only

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Parent/Child try to write:

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- make a copy of the segment and resume

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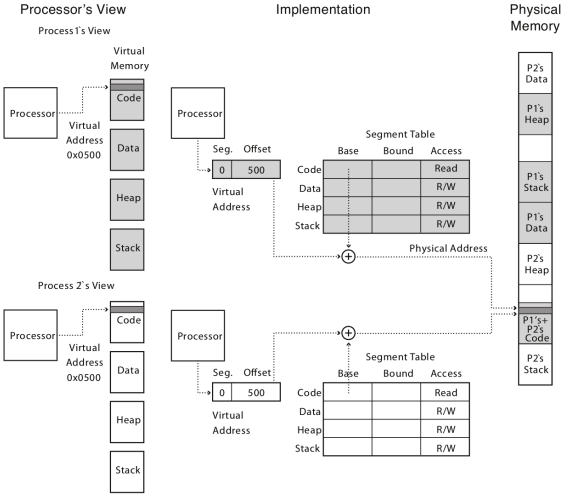

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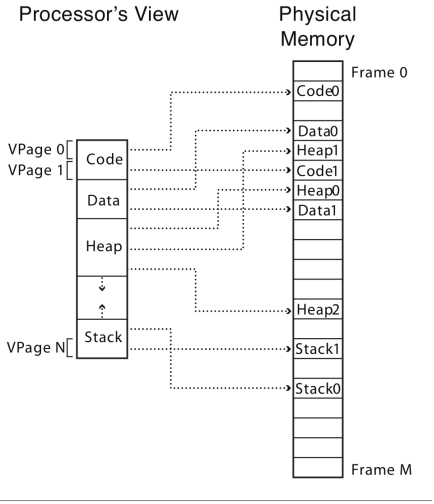
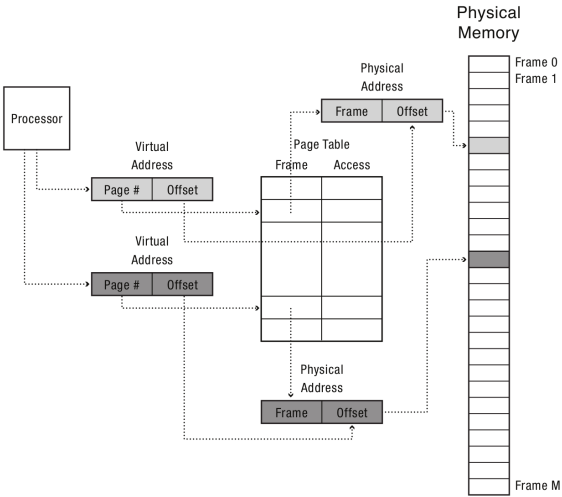
# Logical View of Page Table Address Translation



# paging - implementation



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  - Internal fragmentation: if we don't need all of the space inside a fixed size chunk

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  - Need core map of physical page numbers to track which processes are pointing to which physical page numbers (e.g. *reference count*)

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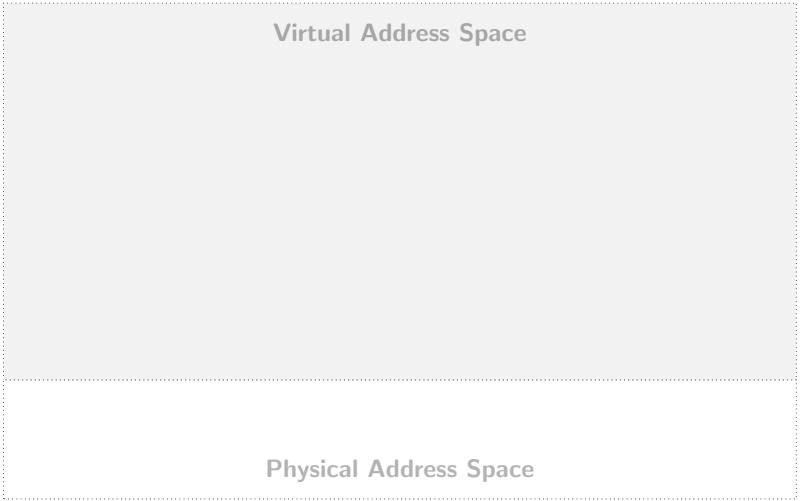

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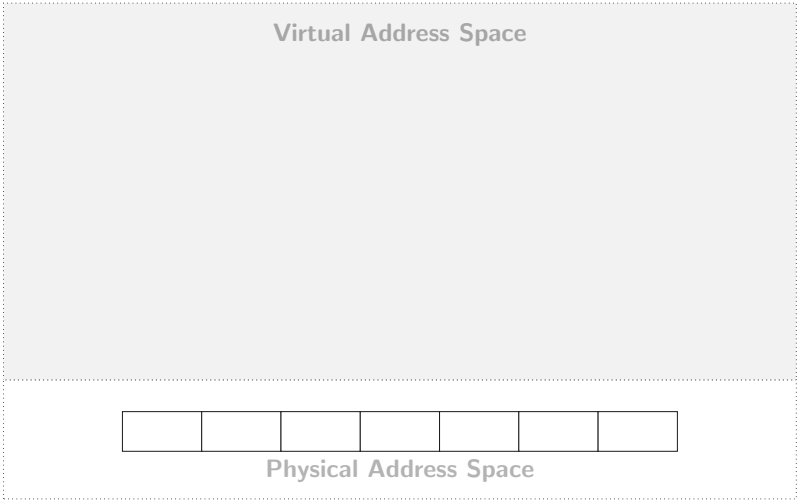

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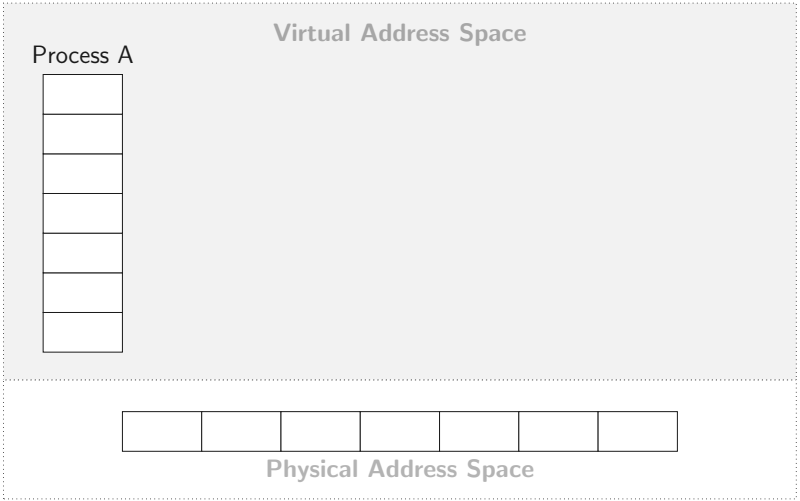

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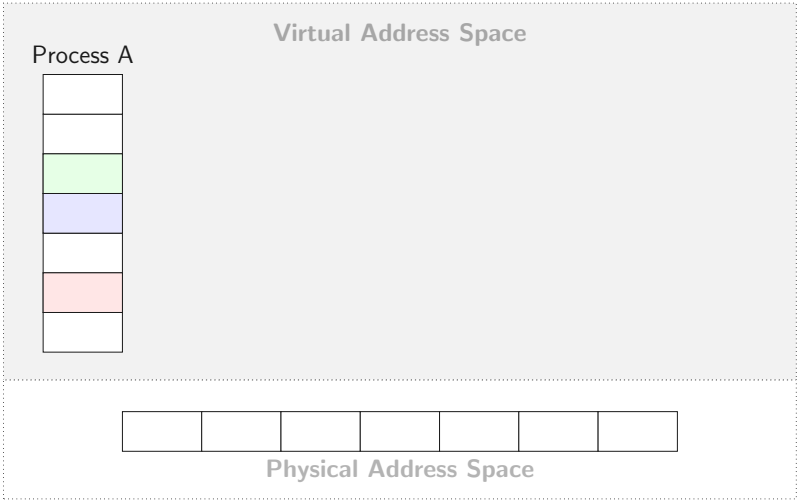

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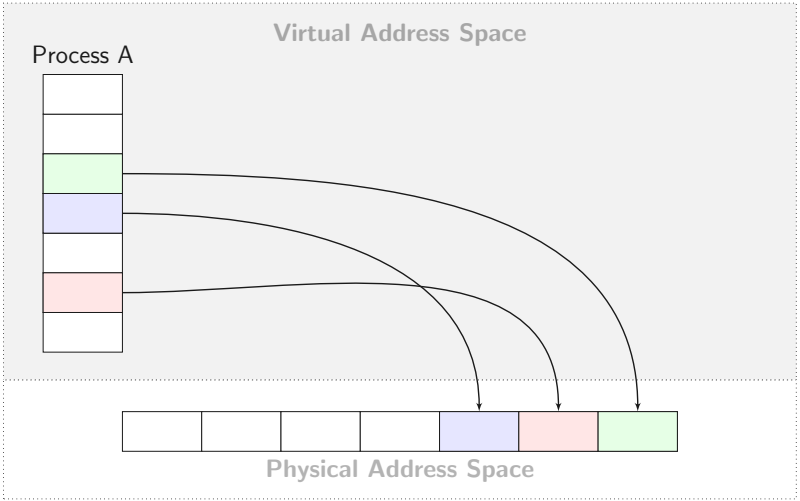

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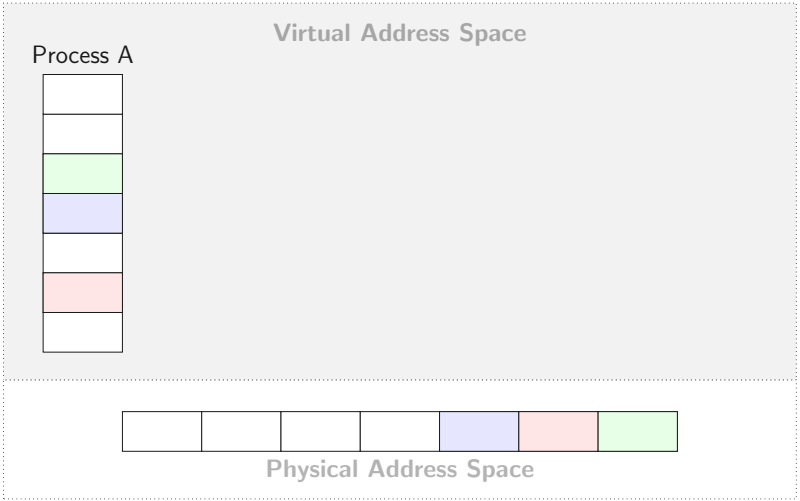

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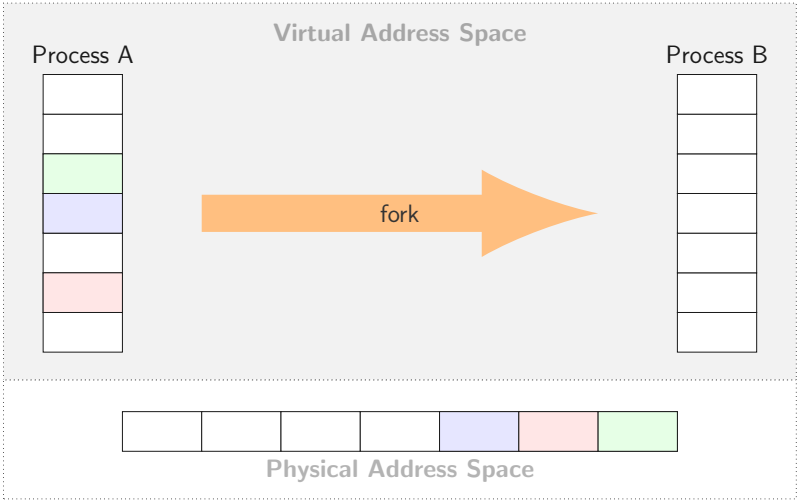

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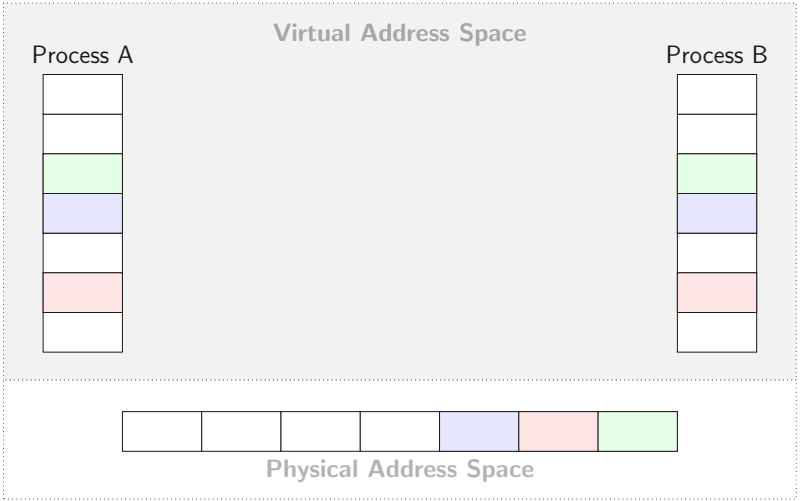

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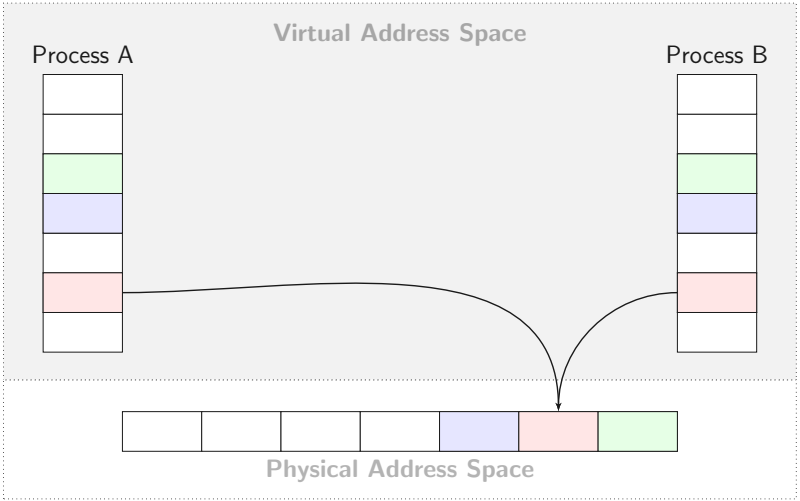

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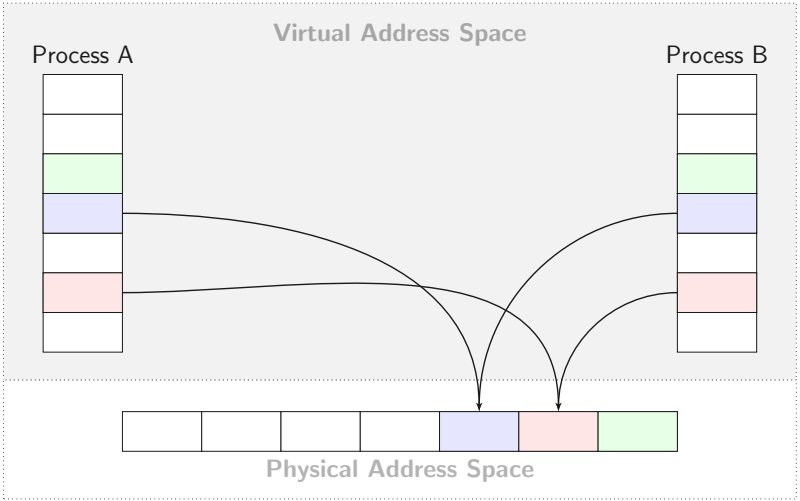

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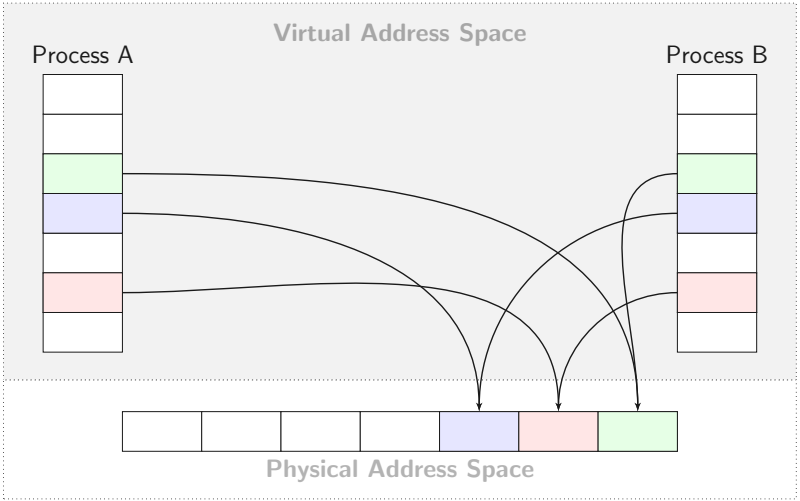

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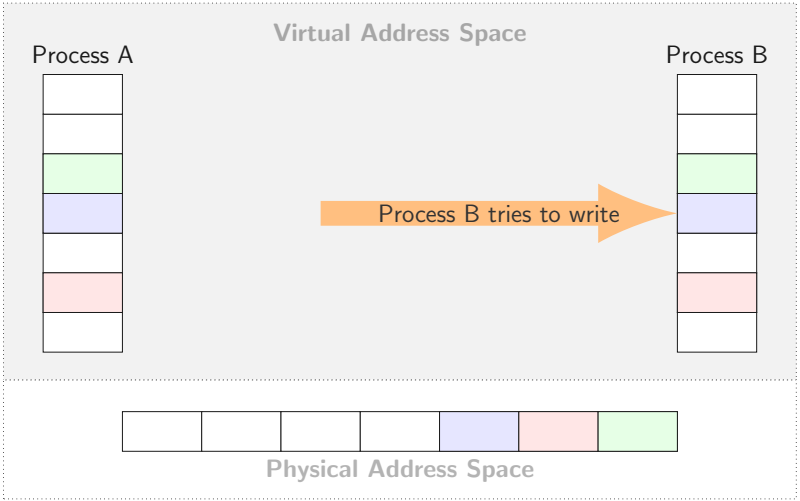

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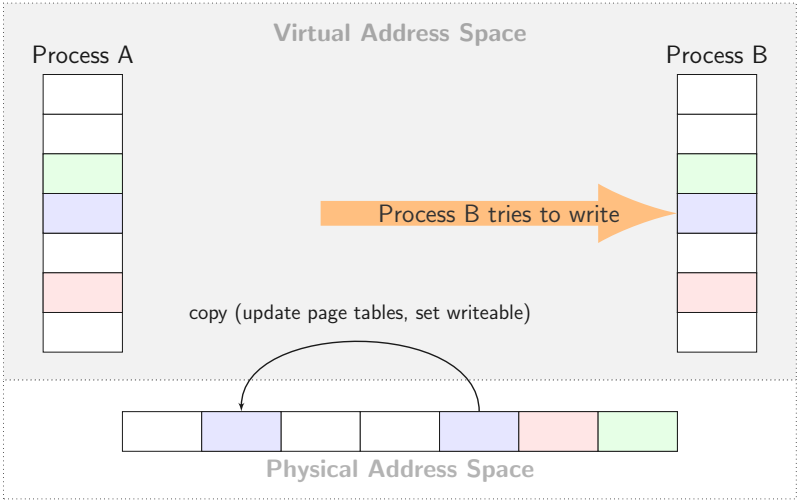

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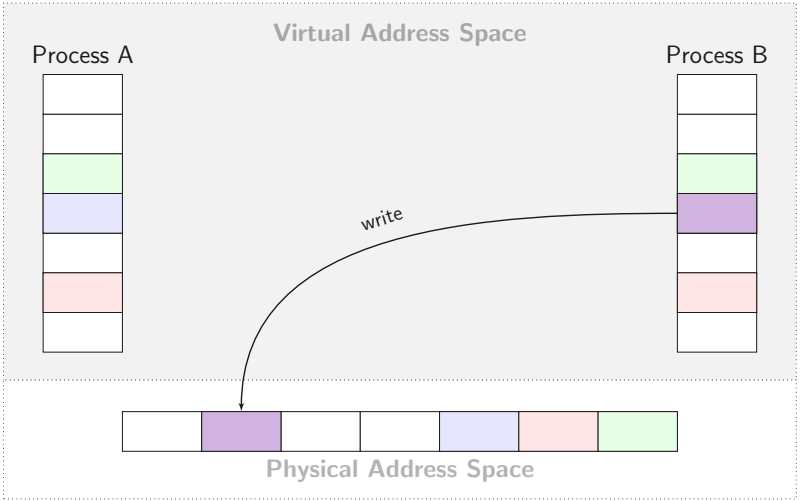

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  - Remaining pages can be transferred in the background while program is running

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- The principle of locality ensures that

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$\rightarrow$ may lower page fault frequency

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- Fixed-size page as lowest level unit of allocation
  - Efficient memory allocation (compared to segments)
  - Efficient for sparse translation tree (compared to simple paging)
  - Efficient disk transfers (fixed size units, page size multiple of disk sector)
  - Easier to build translation lookaside buffers
  - Efficient reverse lookup (from physical $\rightarrow$ virtual)
  - Fine granularity for protection/sharing

# Paged Segmentation

- Process memory is segmented

# Paged Segmentation

- Process memory is segmented
- Segment table entry:

# Paged Segmentation

- Process memory is segmented
- Segment table entry:
  - Pointer to page table

# Paged Segmentation

- Process memory is segmented
- Segment table entry:
  - Pointer to page table
  - Page table length (# of pages in segment)

# Paged Segmentation

- Process memory is segmented
- Segment table entry:
  - Pointer to page table
  - Page table length (# of pages in segment)
  - Access permissions

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  - Access permissions
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  - Access permissions
- Page table entry:
  - Physical page number

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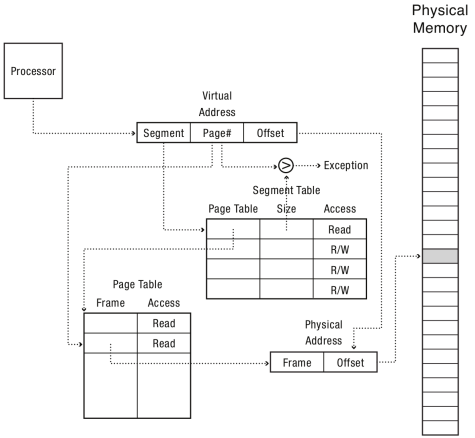
- Page table entry:
  - Physical page number
  - Access permissions

# Paged Segmentation

- Process memory is segmented
- Segment table entry:
  - Pointer to page table
  - Page table length (# of pages in segment)
  - Access permissions
- Page table entry:
  - Physical page number
  - Access permissions
- Share/protection at either page or segment-level

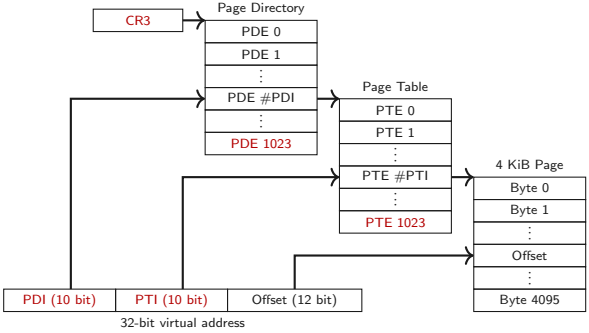
# Paged Segmentation



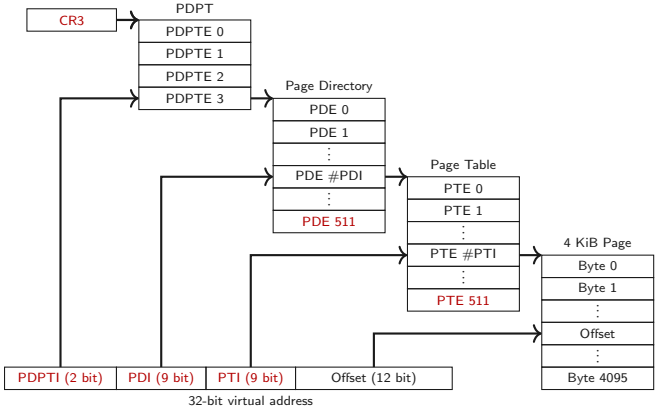
# Question

- With paged segmentation, what must be saved/restored across a process context switch?

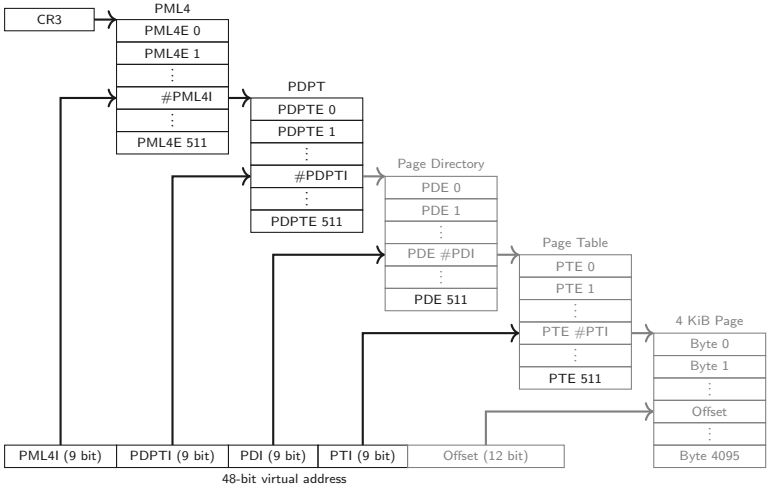
# Paging: x86-32 with page size 4 KiB



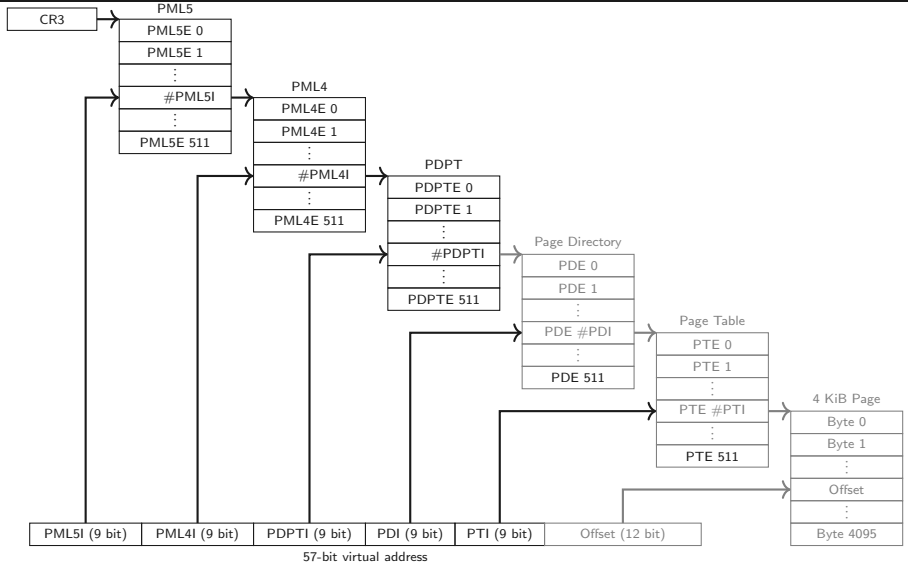
# Paging: x86-32-PAE with page size 4 KiB



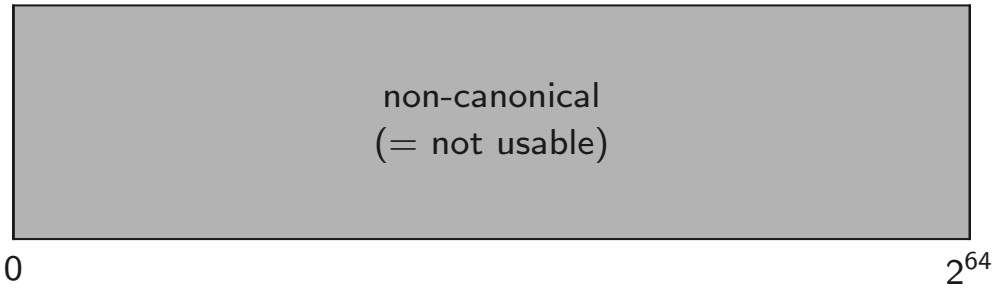
# Paging: x86-64 with page size 4 KiB



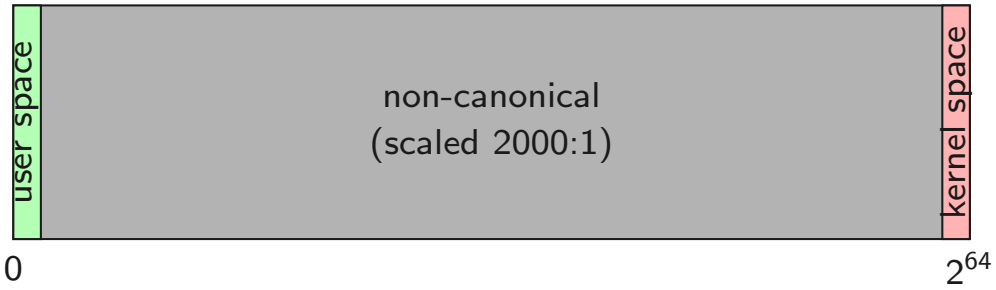
# Paging: x86-64 with PML5 and page size 4 KiB



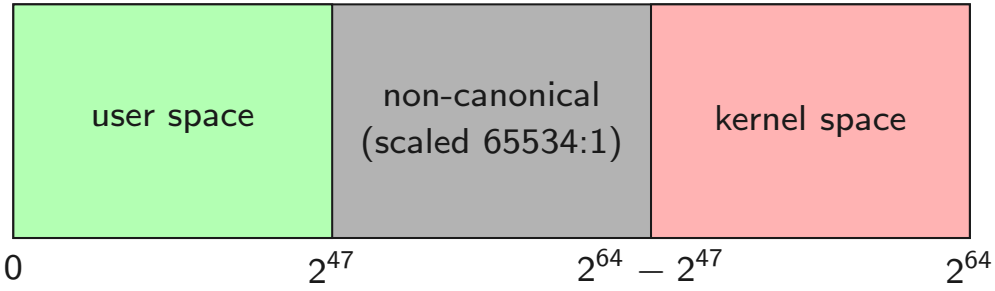
# x86-64 Memory Layout (with PML4)



# x86-64 Memory Layout (with PML4, scaled)



# x86-64 Memory Layout (with PML4, scaled)



# Address Translation on x86 processors

# Intel Pentium

- Segmentation and paging

# Intel Pentium

- Segmentation and paging
- 16 K segments, each 4 GB

# Intel Pentium

- Segmentation and paging
- 16 K segments, each 4 GB
  - Few segments

# Intel Pentium

- Segmentation and paging
- 16 K segments, each 4 GB
  - Few segments
  - Large segments

# LDT - GDT

- Local Descriptor Table LDT

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- Local Descriptor Table LDT
  - for each process

# LDT - GDT

- Local Descriptor Table LDT
  - for each process
  - local segments (Code, Data, Stack)

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- Local Descriptor Table LDT
  - for each process
  - local segments (Code, Data, Stack)
- Global Descriptor Table GDT

# LDT - GDT

- Local Descriptor Table LDT
  - for each process
  - local segments (Code, Data, Stack)
- Global Descriptor Table GDT
  - for system segments

# LDT - GDT

- Local Descriptor Table LDT
  - for each process
  - local segments (Code, Data, Stack)
- Global Descriptor Table GDT
  - for system segments
  - also for kernel

# Segment Registers

- 6 segment registers

# Segment Registers

- 6 segment registers
  - CS: Selector for Code Segment

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- 6 segment registers
  - CS: Selector for Code Segment
  - DS: Selector for Data Segment

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- 6 segment registers
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  - DS: Selector for Data Segment
  - ES: Selector for Data Segment

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  - DS: Selector for Data Segment
  - ES: Selector for Data Segment
  - FS: Selector for Data Segment

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# Segment Registers

- 6 segment registers
  - CS: Selector for Code Segment
  - DS: Selector for Data Segment
  - ES: Selector for Data Segment
  - FS: Selector for Data Segment
  - GS: Selector for Data Segment
  - SS: Selector for Stack Segment

# Segment Selector

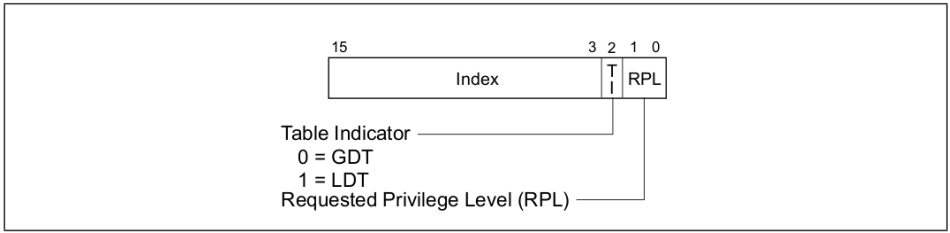



Figure 3-6. Segment Selector

# Segment Selector

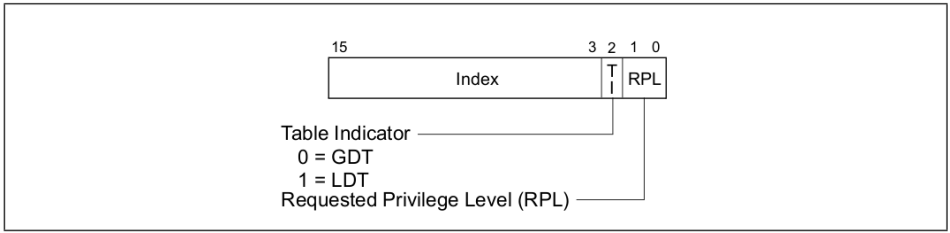



Figure 3-6. Segment Selector

- Null Segment at index 0 → cannot be used

# Segment Selector

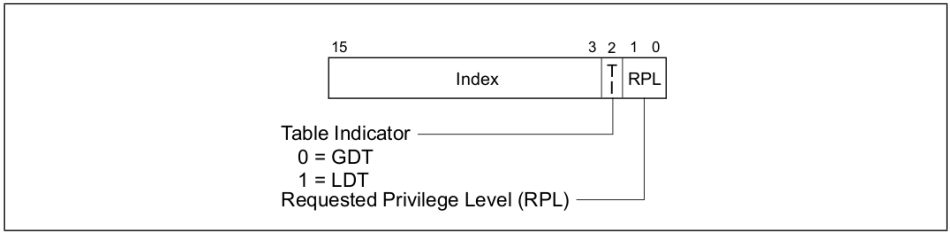



Figure 3-6. Segment Selector

- Null Segment at index 0 $\rightarrow$ cannot be used
- Modifying a segment register loads corresponding descriptor into an internal CPU register

# Hidden Part of Segment Registers

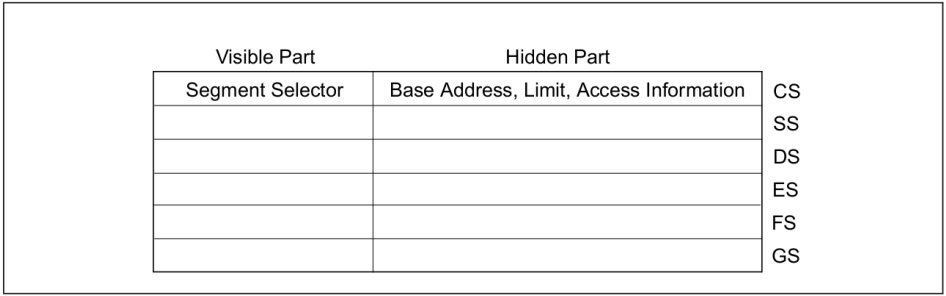
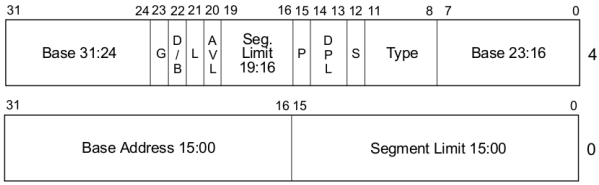



Figure 3-7. Segment Registers

# Segment Descriptor




L — 64-bit code segment (IA-32e mode only)
AVL — Available for use by system software
BASE — Segment base address
D/B — Default operation size (0 = 16-bit segment; 1 = 32-bit segment)
DPL — Descriptor privilege level
G — Granularity
LIMIT — Segment Limit
P — Segment present
S — Descriptor type (0 = system; 1 = code or data)
TYPE — Segment type

Figure 3-8. Segment Descriptor

# Address translation

- we start with (selector, offset)

# Address translation

- we start with (selector, offset)
- CPU looks for correct descriptor in internal registers

# Address translation

- we start with (selector, offset)
- CPU looks for correct descriptor in internal registers
- selector 0 or segment swapped out: interrupt

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  - check limits of course

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- result: linear address

# Address translation

- we start with (selector, offset)
- CPU looks for correct descriptor in internal registers
- selector 0 or segment swapped out: interrupt
- offset exceeds segment size: interrupt
- add base field to offset
  - check limits of course
- result: linear address
- paging turned off: linear address is physical address

# Address translation

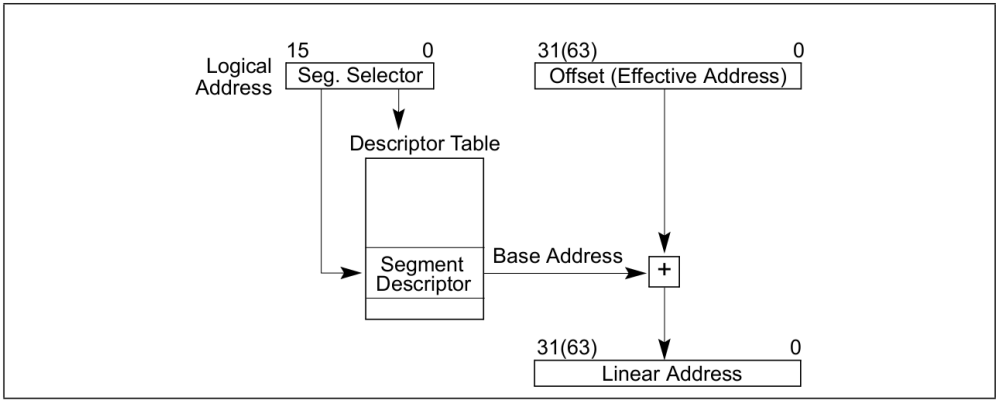


Figure 3-5. Logical Address to Linear Address Translation

# Combining Segments and Paging

OSes today have only a very small number of segments:

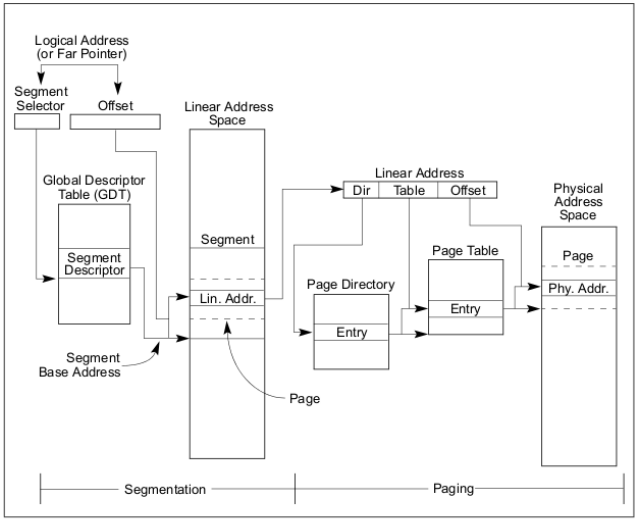


Figure 3-1. Segmentation and Paging

# Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code

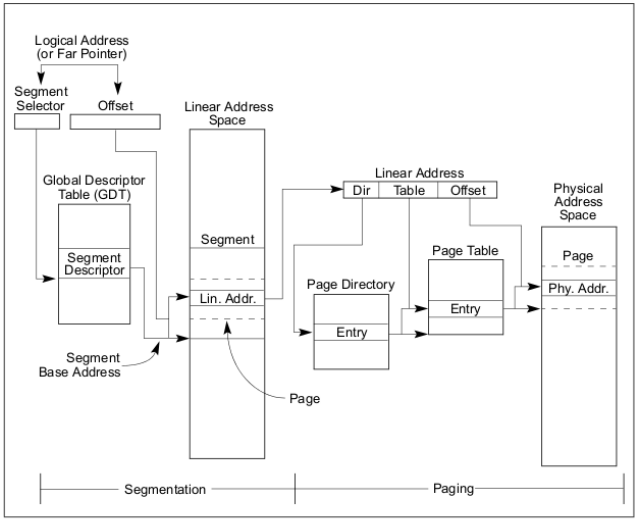


Figure 3-1. Segmentation and Paging

# Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code
- 1 for user data

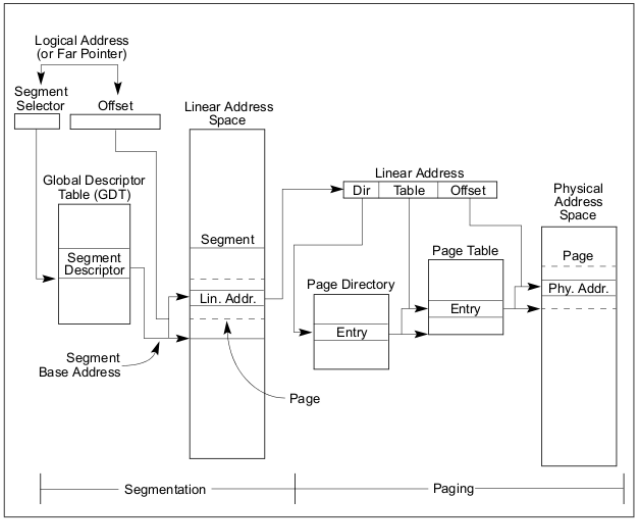


Figure 3-1. Segmentation and Paging

# Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code
- 1 for user data
- 1 for user thread local storage

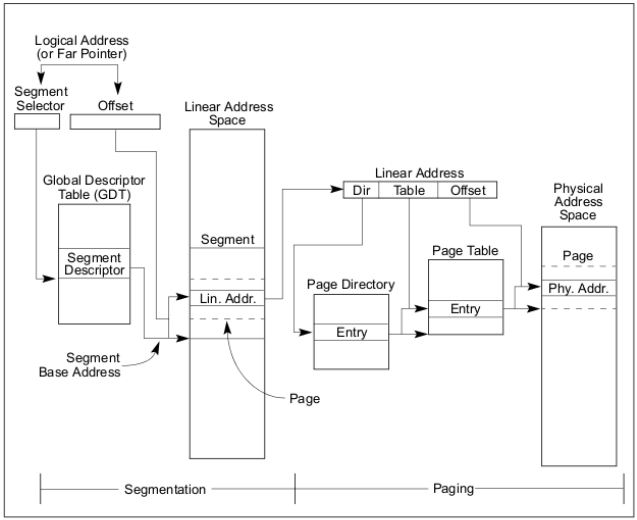


Figure 3-1. Segmentation and Paging

# Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code
- 1 for user data
- 1 for user thread local storage
- 1 for kernel code

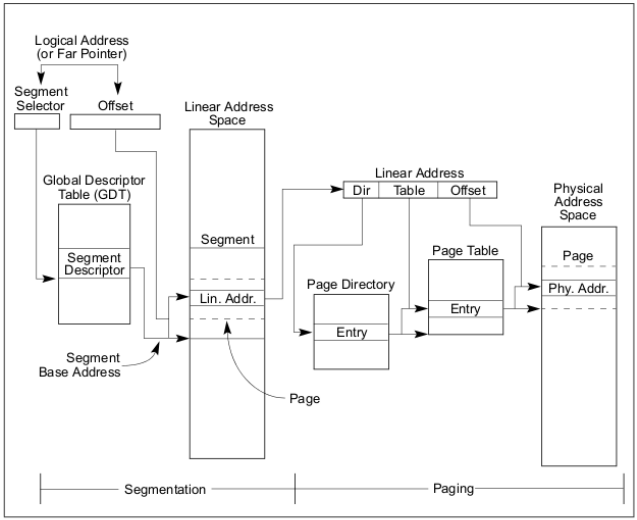


Figure 3-1. Segmentation and Paging

# Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code
- 1 for user data
- 1 for user thread local storage
- 1 for kernel code
- 1 for kernel data

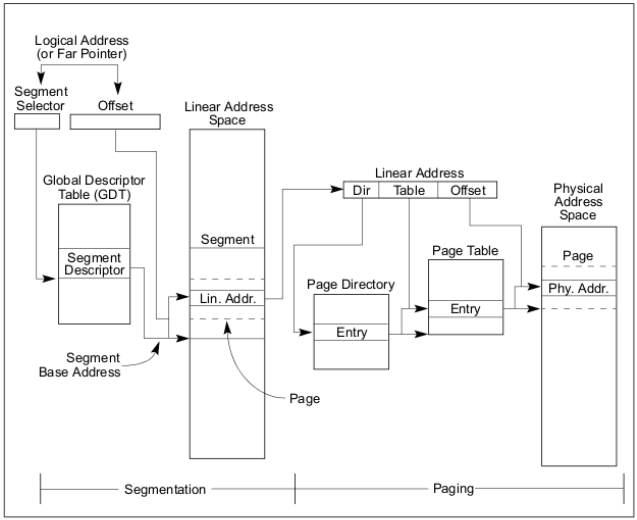


Figure 3-1. Segmentation and Paging

# Combining Segments and Paging

OSes today have only a very small number of segments:

- 1 for user code
- 1 for user data
- 1 for user thread local storage
- 1 for kernel code
- 1 for kernel data
- 1 for kernel core local storage

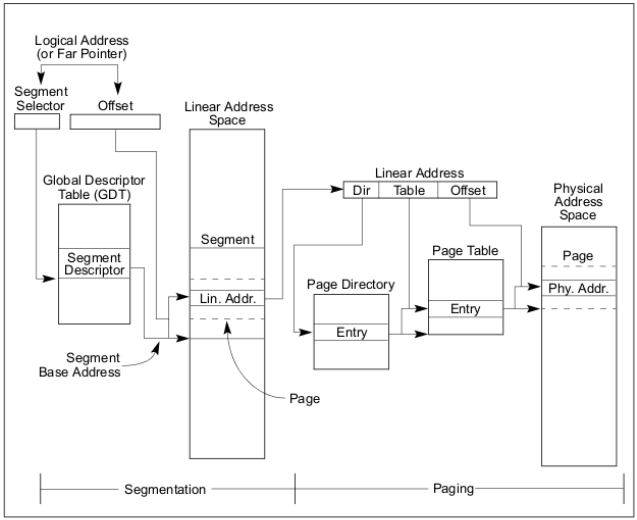


Figure 3-1. Segmentation and Paging

# Segments Today

- x86-64 requires segment base to be 0 and limit to be unlimited

# Segments Today

- x86-64 requires segment base to be 0 and limit to be unlimited
- not even used anymore to separate code and data

# Segments Today

- x86-64 requires segment base to be 0 and limit to be unlimited
- not even used anymore to separate code and data
- most OSes today only use segments to determine the privilege level

# Take Aways

Virtual memory

# Take Aways

Virtual memory

- is based on Segmentation and Paging

# Take Aways

Virtual memory

- is based on Segmentation and Paging
- enables effective protection mechanisms

# Take Aways

Virtual memory

- is based on Segmentation and Paging
- enables effective protection mechanisms
- enables sparse address spaces