SCIENCE
PASSION
TECHNOLOGY

Digital System Integration and Programming

Barbara Gigerl, Rishub Nagpal

October 4th, 2023

Outline

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What is digital system integration and programming?

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- System integration: connect multiple complex systems to achieve a certain goal

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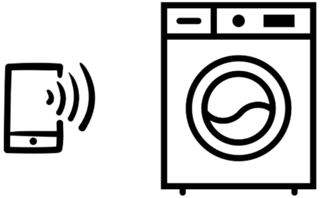

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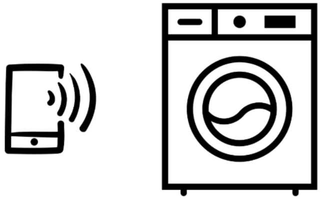

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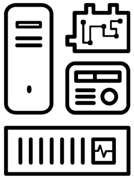

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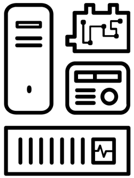

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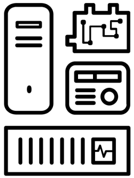

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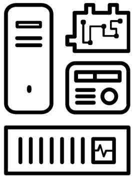

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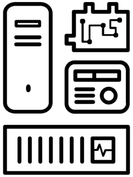

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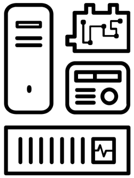

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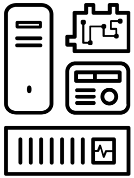

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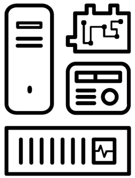

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- Today: SoC is the state-of-the-art principle for designing chips

SoCs are everywhere

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Tablets

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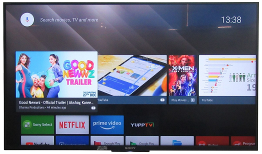
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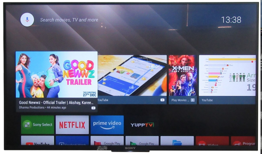
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  - SPU: dedicated subsystem for boot-loader, key management unit, crypto accelerators, ...

Example: Sitara Processors of TI

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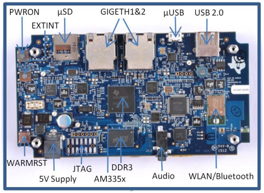

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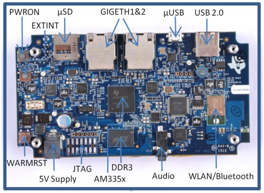

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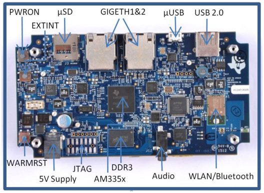

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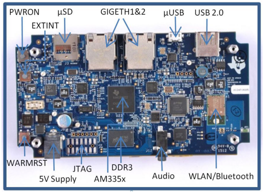

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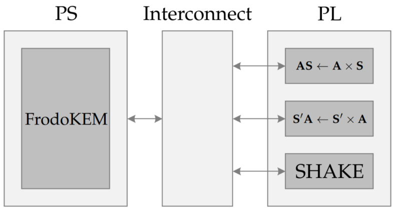
PS
Interconnect
PL
FrodoKEM
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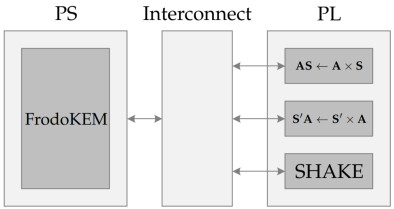
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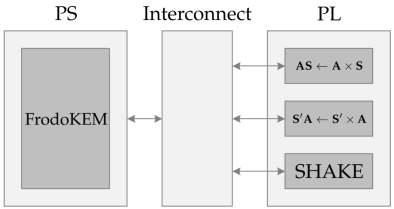
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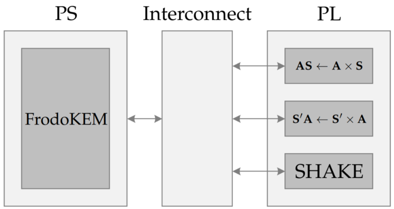

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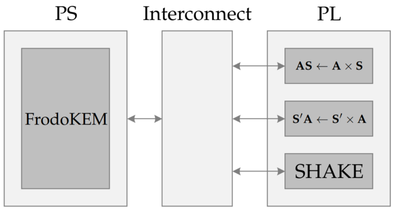

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- Costa et al. [CLR22]
  - ARM processor: FrodoKEM
  - FPGA: SHAKE128 hash function which is part of FrodoKEM

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- A bus connecting all components: AMBA, AXI, CoreConnect, ...

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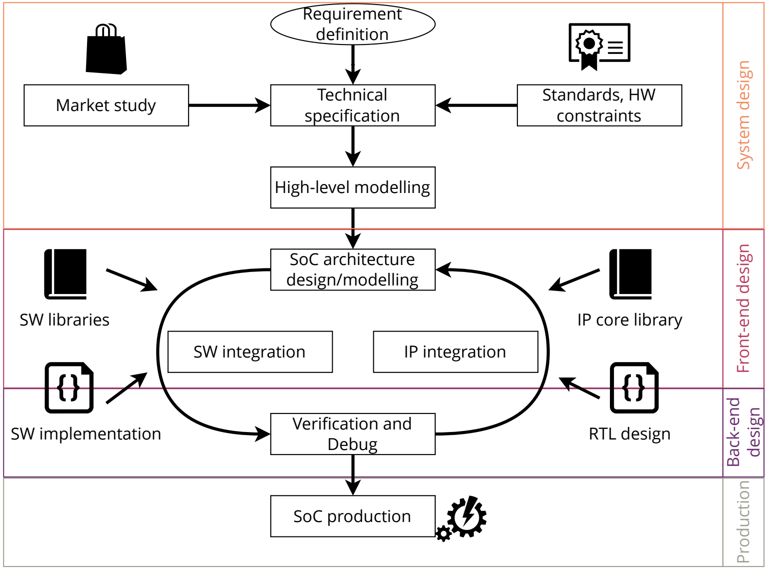
SoC Design Methodology



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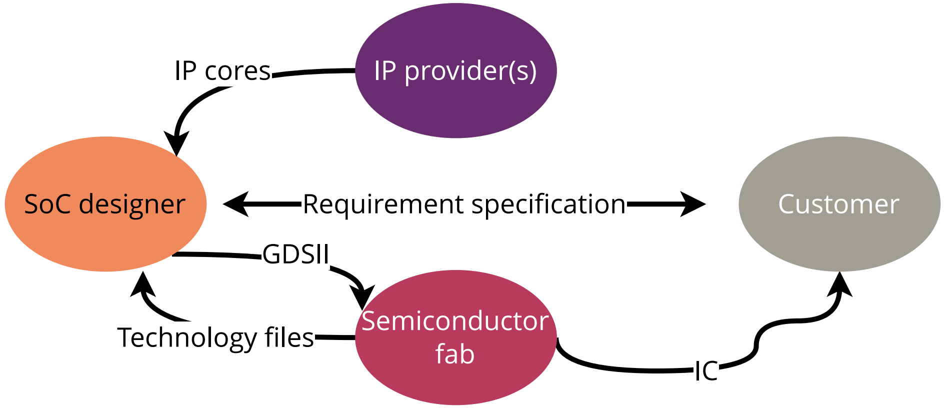

- GDSII: data format to describe ICs
- Technology file: information about manufacturing (metals, IC layers, ...)

Who are we?

Barbara Gigerl

PhD student @ Graz University of Technology

Formal Verification of Side-Channel Protected Implementations

✉ barbara.gigerl@iaik.tugraz.at

✉ sip-team@iaik.tugraz.at

Who are we?

Rishub Nagpal

PhD student @ Graz University of Technology

Power side-channel attacks and defenses for cryptographic implementations

✉ rishub.nagpal@iaik.tugraz.at

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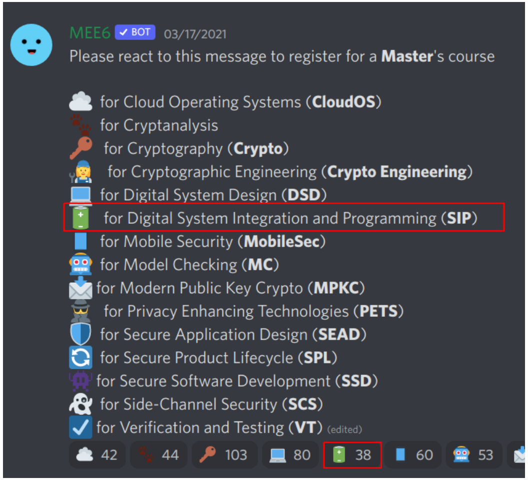
  mailto:sip-team@iaik.tugraz.at
- Questions and concerns via Discord
  https://discord.gg/9KKGfndsD5
- Come by our office (IF01052 and IF01060)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for Cryptanalysis
for Cryptography (**Crypto**)
for Cryptographic Engineering (**Crypto Engineering**)
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for Digital System Integration and Programming (**SIP**)
for Mobile Security (**MobileSec**)
for Model Checking (**MC**)
for Modern Public Key Crypto (**MPKC**)
for Privacy Enhancing Technologies (**PETS**)
for Secure Application Design (**SEAD**)
for Secure Product Lifecycle (**SPL**)
for Secure Software Development (**SSD**)
for Side-Channel Security (**SCS**)
for Verification and Testing (**VT**) (edited)

42 44 103 80 38 60 53

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- Active communication within your group
- Active participation, presence during lectures

Teaching method

We expect:

- Investment of time
  - SIP: 3 VU (5 ECTS)
  - $5 \times 25 = 125$ hours work = 28 days of 8 hours
- Active communication within your group
- Active participation, presence during lectures
  - *Courses with continual assessment (UE, VU, SE, etc.) are subject to compulsory attendance (§ 15 of the Statute part Legal Regulations for Academic Affairs).*

Grading

Your grade consists of:

- Project 1: 20%

Grading

Your grade consists of:

- Project 1: 20%
    - Individual work, independent submissions

Grading

Your grade consists of:

- Project 1: 20%
  - Individual work, independent submissions
- Project 2: 50%

Grading

Your grade consists of:

- Project 1: 20%
  - Individual work, independent submissions
- Project 2: 50%
  - Team work in groups of 3-4 students

Grading

Your grade consists of:

- Project 1: 20%
  - Individual work, independent submissions
- Project 2: 50%
  - Team work in groups of 3-4 students
- Seminar presentation: 30%

Grading

Your grade consists of:

- Project 1: 20%
  - Individual work, independent submissions
- Project 2: 50%
  - Team work in groups of 3-4 students
- Seminar presentation: 30%
  - Selection from course catalog OR suggest your own topic

Grading

Your grade consists of:

- Project 1: 20%
  - Individual work, independent submissions
- Project 2: 50%
  - Team work in groups of 3-4 students
- Seminar presentation: 30%
  - Selection from course catalog OR suggest your own topic
  - Slides are reviewed by us (submit until Monday evening)

Grading

Your grade consists of:

- Project 1: 20%
  - Individual work, independent submissions
- Project 2: 50%
  - Team work in groups of 3-4 students
- Seminar presentation: 30%
  - Selection from course catalog OR suggest your own topic
  - Slides are reviewed by us (submit until Monday evening)
- Bonus points for questions during/after seminar presentations

Team work

- Team Size for Project 1: 1
- Team Size for Project 2:
    - Group size = Number of Participants / Number of Boards = 27 / 8
    - 5 groups of 3, 3 groups of 4
- Team Size for Seminar presentation: 1

Registration Process

1. Find a group
2. Register your group: `sip-team@iaik.tugraz.at`
3. Wait for the confirmation mail to get your group number
4. Choose a seminar topic
5. Register for a seminar topic: `https://www.termino.gv.at/meet/b/96af1b7b54cbfe4fbfbcdb4a2bb94788-256179`
6. Receive your git repositories (by email)

Deadline: Monday, 9.10., 23:59

Schedule of SIP 2022

Sessions

- Regular weekly sessions: Wednesday 10:00 - 12:00, IFEG042

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  1. Seminar talk + discussion
  2. Seminar talk + discussion
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  4. Everyone briefly (1-2 sentences) comments on own project progress

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- Regular weekly sessions: Wednesday 10:00 - 12:00, IFEG042
- Program for each session
  1. Seminar talk + discussion
  2. Seminar talk + discussion
  3. Seminar talk + discussion
  4. Everyone briefly (1-2 sentences) comments on own project progress
  5. Questions, problems about the project

Preliminary timeline

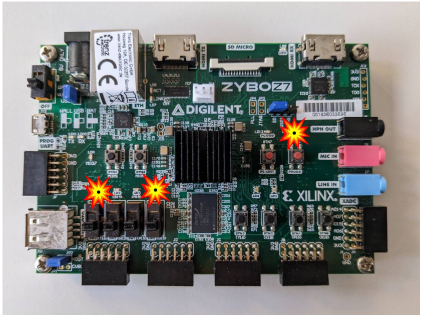
Date	Topic
04.10.	Kick-off / Introduction to Seminar Topics / SoC Design Flow Tutorial
11.10.	Embedded Linux Tutorial / Presentation Project 1
18.10.	Debugging Tutorial
25.10.	Q&A Project 1
1.11.	Public holiday (no meeting)
8.11.	Seminar talks + Q&A
15.11.	Presentation Project 2a+2b / Seminar talks + Q&A
22.11.	Seminar talks + Q&A
29.11.	Seminar talks + Q&A
6.12.	Seminar talks + Q&A
13.12.	Seminar talks + Q&A
10.01.	Seminar talks + Q&A
17.01.	Seminar talks + Q&A
24.01.	Seminar talks + Q&A

Important Dates and Deadlines

Date	**Topic**
9.10., 23:59	Deadline Group Registration
14.11., 23:59	Deadline Project 1
15.11.-17.11.	Exercise Interviews Project 1
12.12., 23:59	Deadline Project 2a
13.12.-15.12.	Exercise Interviews Project 2a
23.01., 23:59	Deadline Project 2b
24.01.-26.01.	Exercise Interviews Project 2a

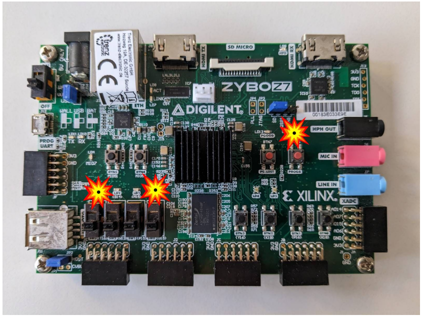
Project 1: Fancy Lights

- Get to know the board and run through all steps



Project 1: Fancy Lights

- Get to know the board and run through all steps
- Design hardware, build a driver, write an application



Project 1: Fancy Lights

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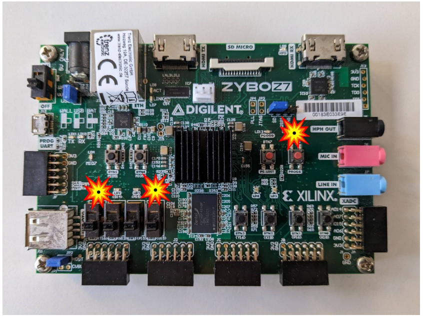

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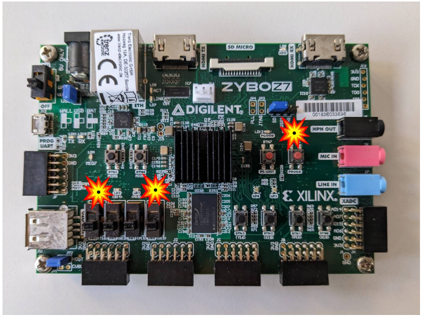
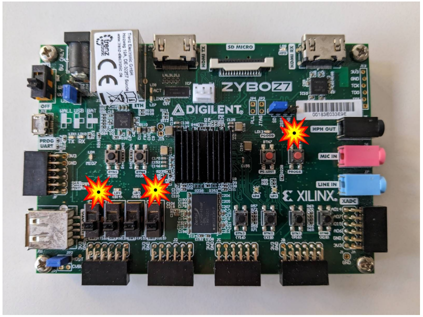


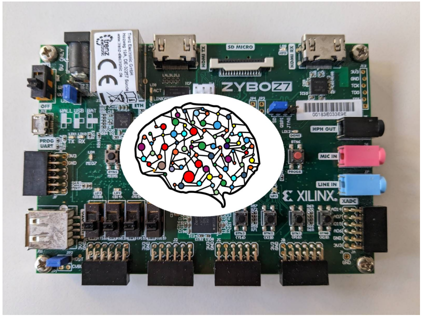
Project 1: Fancy Lights

- Get to know the board and run through all steps
- Design hardware, build a driver, write an application
- Access the LEDs from a bare-metal application and from within Linux
- No team work; everybody should do all steps (share your board within group)
- Aim: After completing, everybody should have the same basic knowledge.



Project 2: FPGA-based image classification

- Use knowledge from Project 1 to build larger system



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- Use knowledge from Project 1 to build larger system
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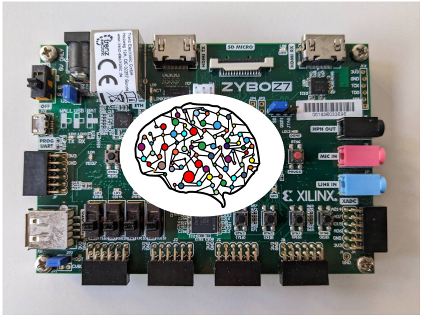

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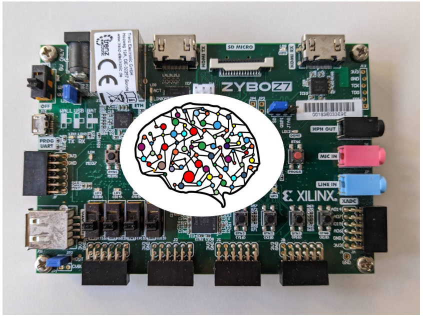

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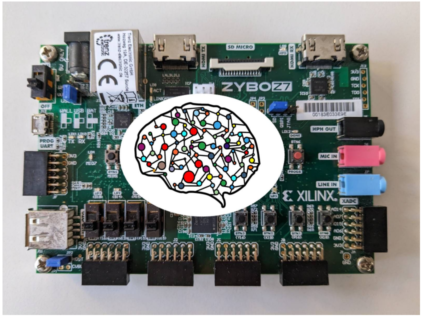

Project 2: FPGA-based image classification

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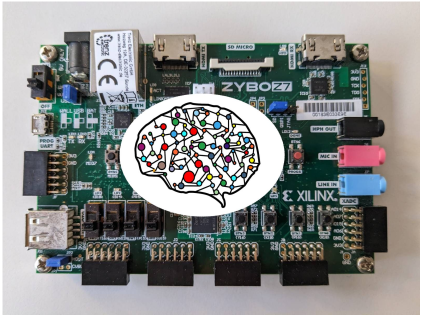
- FPGA runs NN to classify images from the MNIST test dataset
- Receive image via Ethernet - send to NN - return classification result to correct user
- Team work
- Aim: Get some deeper understanding of the topic



References I

[CLR22] Vinicius Lagrota Rodrigues da Costa, Julio Lopez, and Moises Vidal Ribeiro. **A System-on-a-Chip Implementation of a Post-Quantum Cryptography Scheme for Smart Meter Data Communications.** Sensors 22.19 (2022), p. 7214. DOI: 10.3390/s22197214. URL: https://doi.org/10.3390/s22197214.