FPGAs in Space

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Overview

- History
- Challenges in space
- Problems caused by radiation
- Mitigations
- Manufacturers of space qualified FPGAs
- Lessons learned

History

First FPGA in space

- Used in data processing unit of SAMPEX spacecraft in *1992*
- Six A1020 chips for redundancy
- 547 logic cells

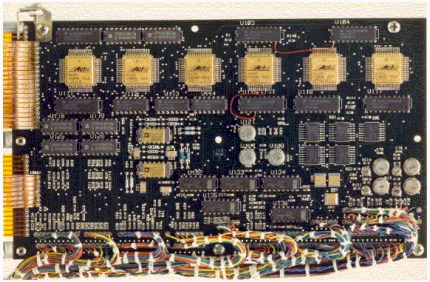

Figure 1: Sampex data processing unit [2]

Why use FPGA in space?

- Space missions are getting more and more complex
- Comparison to microcontrollers:
  - More efficient in energy and space consumption
  - *Higher computing power* (parallelism)
  - More expensive, longer development times
- Comparison to ASICs:
  - Less efficient in energy and space consumption
  - Less computing power
  - *Less expensive*, shorter time to launch
- Conclusion: FPGAs are the *sweet-spot between ASICs and μCs*

FPGA vs. ASIC per mission

- Immarsat 4: Communication satellite, launched in 2008
- Bepicolombo: Orbiter, launched in 2018

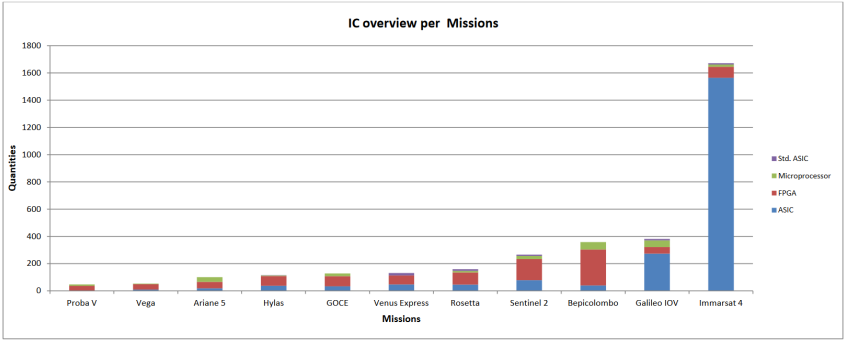

Figure 2: ICs per space mission [1]

FPGA vs. ASIC over time

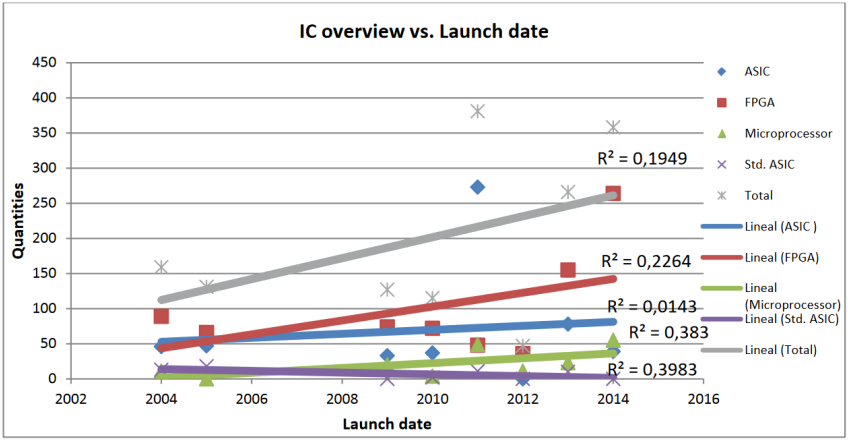

Figure 3: IC overview vs. launch date [1]

IC usage vs. cost

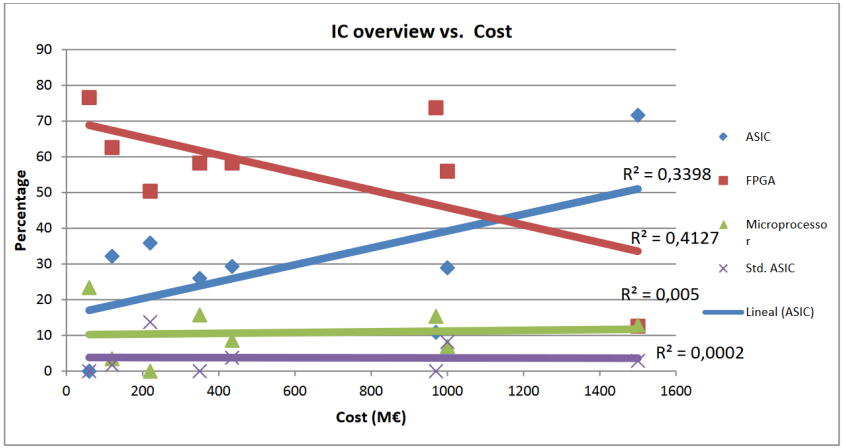

Figure 4: IC usage vs. cost [1]

Challenges in space

Challenges in space

- Exposure to radiation
- Temperature
- Weight and space limits
- Power consumption

Radiation

- Emitted by the sun
- *Non-ionizing* radiation can be shielded by the right materials
- *Ionizing* radiation can't be shielded, charged particles travel through substances
- Change in behaviour of semiconductors

Problems caused by radiation

Long term effects

- High-energy ionizing radiation creates *electron holes within the oxide* of MOS transistors.
- Charge is built up within the oxide
- Changes in *threshold voltage* and timing
- Might lead to total failure

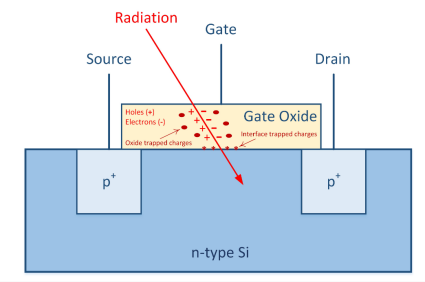

Figure 5: Radiation in MOS oxide [3]

Single event latchup (SEL)

- CMOS has *intrinsic transistors in substrate*
- Creates *latch-up circuit*
- Radiation might trigger the latch-up
- Low impedance connection between V_{dd} and *gnd* leads to *permanent damage*

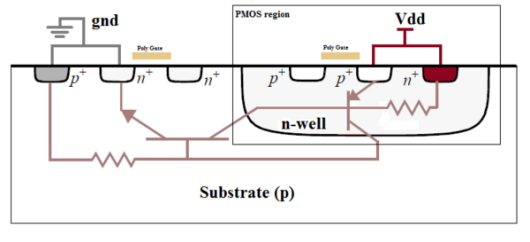

Figure 6: Latch-up circuit in CMOS [4]

Single event upset (SEU)

- When radiation passes through device, charge is transferred between nodes
- If critical charge is exceeded, a *change in voltage level* happens
- This results in a *bitflip*
- Temporal error

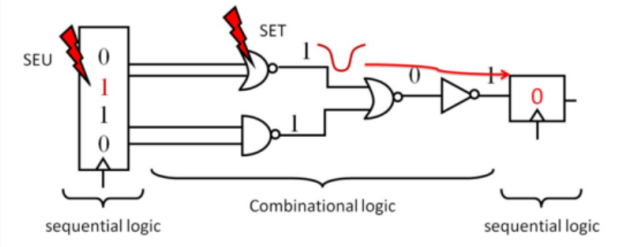

Figure 7: Example of SEU in combinational logic [5]

FPGA architecture vulnerabilities

- Because of its large space consumption, *memory is very vulnerable* to bitflips
- Especially upsets in *configuration memory*, which takes most of the memory space, will lead to different logic behaviour
- Types of configuration memory:
  - Antifuse: only programable once, immune to SEU
  - Flash: limited programming cycles, immune to SEU
  - *SRAM*: unlimited programming cycles, vulnerable to SEU

FPGA Architecture Vulnerabilities

- Example bitflip in configuration memory:

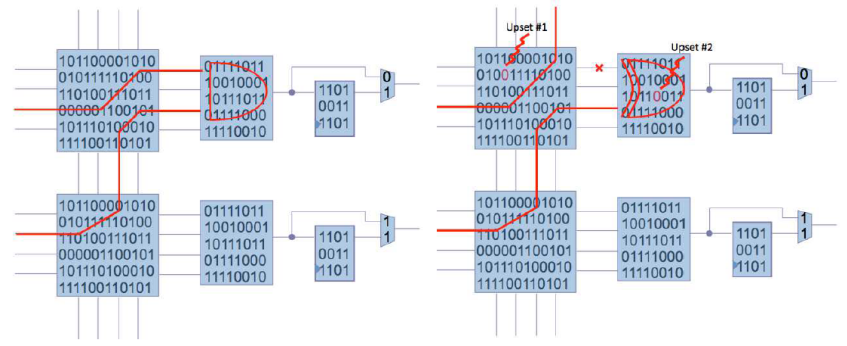

Figure 8: Bitflip example [6]

Mitigations

Triple modular redundancy (TMR)

- Can be realized within single FPGA or on three seperate FPGAs
- Single SEU allowed in one branch
- *Big overhead* in space and power consumption

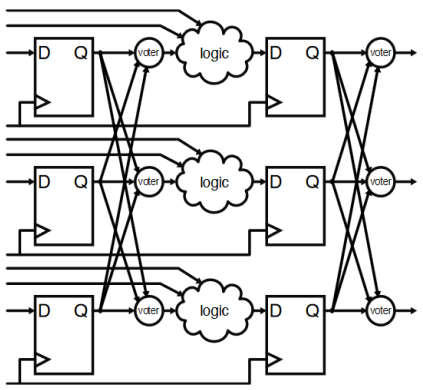

Figure 9: Triple modular redundancy [6]

Configuration scrubbing

- Frequently check integrity of configuration in SRAM by comparing to source memory
- Repair upsets when difference is noticed
- No guarantee for protection against temporal errors
- Often used in combination with TMR

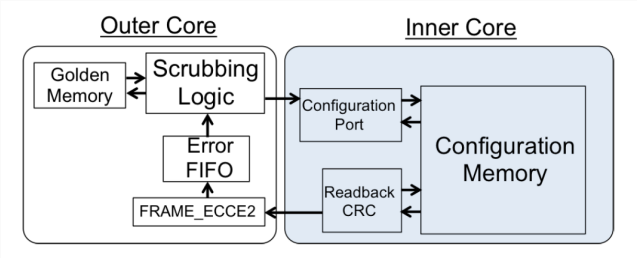

Figure 10: Hybrid scrubbing [7]

Protection on physical level

- Special manufacturing processes for MOS technology
- *Thinner oxide* to reduce probability of electron holes
- *Isolating wells* from the substrate to prevent latch-up
- Different *transistor shapes and sizes*

Manufacturers of space FPGAs

Overview of Space Graded IC Manufacturers

ASIC	FPGA	Microprocessor	Standard ASIC
Aeroflex	ACTEL (Microsemi)	Aeroflex	Aeroflex
AMIS	Aeroflex	ATMEL	ATMEL
ATMEL	ALTERA	DYNEX	DYNEX
Honeywell	ATMEL	FREESCALE	HONEYWELL
INFINEON	XILINX	HONEYWELL	IBM

Figure 11: IC manufacturers for space application [1]

- Radiation Tolerant (RT) Kintex UltraScale XQRKU060
  - First 20nm (predecessor was 65nm) FPGA for space applications
  - 726000 (predecessor had 81900) logic cells
  - 38Mb (predecessor had 12Mb) of memory
  - Uses TMR and external scrubbing

Symbol	Description	Min	Typ	Max	Units
TID	Total Ionized Dose (GEO)	-	100	120	Krad (Si)
SEL	Single-Event-Latch-Up Immunity	-	80	-	MeV-cm2/mg
SEUCRAM	Single-Event Upset in Configuration RAM (GEO)	-	1.0e-8	-	Upset/bit/day
SEUBRAM	Single-Event Upset in Block RAM (GEO)	-	8.5e-9	-	Upset/bit/day
SEFICRAM	Single Event Functional Interrupt Orbital Upset Frequency – Configuration RAM (GEO)	-	4.5e-4	-	Upset/device/day

Figure 12: Radio tolerance of QRKU060 [8]

Microchip

- RT PolarFire
  - 28nm process technology
  - 481000 logic cells
  - 33Mb of memory
  - Synthesis support for TMR and scrubbing
- Radiation tolerance:
  - 100 *Krad* total ionizing dose
  - No SEUs in configuration memory
  - Data upset rate of $10^{-10} errors/bit/day$

Lessons learned

The WIRE power-up mishap [9]

- NASA Wide Field Infrared Explorer (WIRE) spacecraft was launched in 1999
- Synchronous reset to force FPGA logic into a *safe state*
- Start-up time of *crystal oscillator* was not considered
- Circuit was in non-deterministic state during this time
- Problem: lack of documentation of FPGA behaviour, default states were not considered
- WIRE went out of hydrogen and could not perform operations

ESA FPGA Task Force [10]

- In 2001 European Space Agency (ESA) set up task force to perform investigations on FPGA implantations
- Results:
  - Designers unaware of how synthesis tools work
  - Little effort in *testing of SEU* correction implementation
  - *Lack of documentation* for FPGA behaviour
  - Reviews on completed designs are extremely costly

Conclusion

- FPGAs have been in space since 1990s
- Trends show *rise* in FPGA vs. ASIC use
- FPGA chips need to be protected against radiation:
  - On physical level (transistors, shielding)
  - Single event correction: TMR, scrubbing, ECC
- Manufacturers improving technologies
- Mistakes made in the past

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