Network on a chip

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Outline

Introduction

“Route packets, not wires!”

NoC routing & switching

Challenges

Implementations

Introduction

A short history of computing devices

- 1970s: Room- to rack-level systems
- 1980s: Rack- to board-level systems
- 1990s: Board- to chip-level systems
  - System-on-chip
- What is the next step?

Intra-SoC communication

- Connecting different IP cores
- SoC rely on: [1]
  - Central bus or multi-bus
  - Point-to-point connections

SoC communication structures

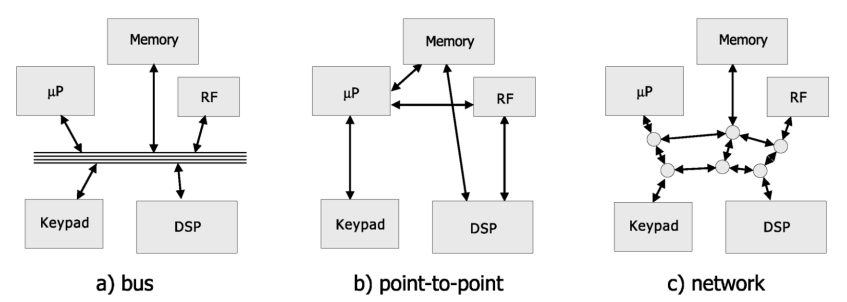

Figure 1: SoC communication structures [2]

Relative delay vs. increasing technology

With smaller technologies:

- Gate delays decrease
- Local wire delays decrease
- Global wire delays **increase**

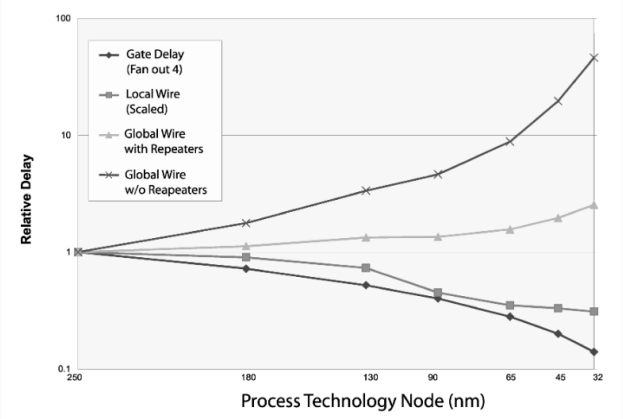

Figure 2: Relative delay vs process technology node [2]

Intra-SoC bus communication problems

- SoC technology advances: computation gets cheaper & communication gets harder [2]
  - Every IP core attached to bus adds parasitic capacity
  - Smaller technologies increase delay via bus
  - Bottleneck bus arbitration
  - Bandwidth limited/shared for all bus nodes
  - Bus timing gets harder (synchronization of whole chip)
- Idea: use concepts of computer networks for SoCs: **network-on-chip**

“Route packets, not wires!”

What is NoC?

- More than one definition [2]
- NoC is a subset of SoC
  - Data-forwarding communication structure
- NoC is an extension of SoC
  - Broader definition, also including application and system architecture

Basic ideas of NoCs [2]

- \+ Switching network as a main communication topology in SoC
- \+ Point-to-point connections between routers
- \+ Local performance not affected by scaling
- \+ Pipelining possible as point-to-point connections between routers
- − Overhead for network switching and contention
- − Wrapper for some IP cores necessary

NoC communication structure

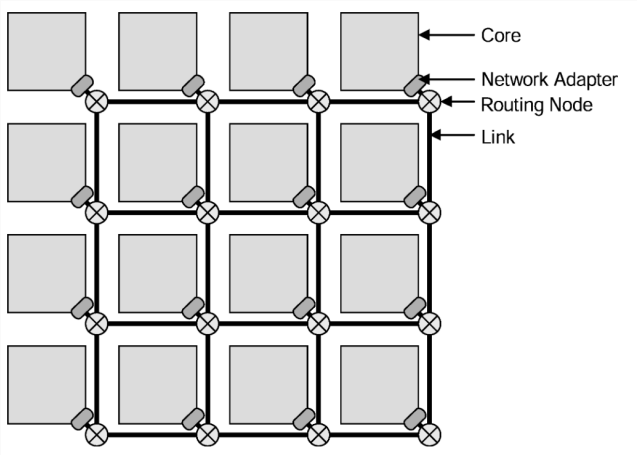

Figure 3: NoC communication structure [2]

NoC topologies

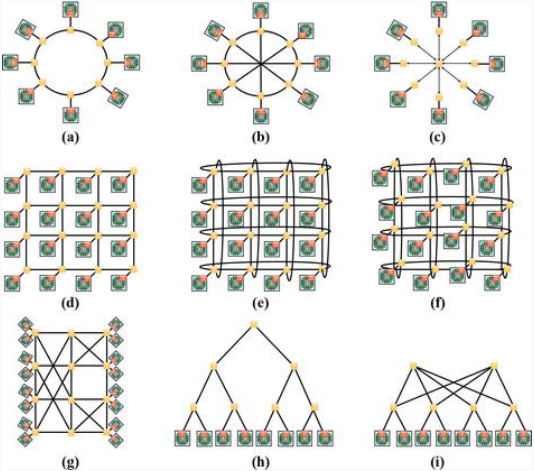

Figure 4: Different NoC topologies [3]

NoC routing & switching

Routing [3]

- Static routing
  - Fixed paths between sources and destinations
  - Simple router logic
  - Router load not considered
- Dynamic routing
  - Routing decisions based on current state of network
  - Traffic can be routed more efficiently
  - Limited effectiveness due to limited knowledge of global network state
  - Complex router logic

Switching [3]

- Circuit switching
  - Establishing physical path between source and destination
  - Low latency transfers
  - Full bandwith utilization leads to wasted links
- Packet switching
  - No link reservation
  - Different packets, different delays
  - Quality of service difficult to guarantee (contention)

Flow control [4]

- Controls how network resources are allocated
- Bufferless flow control
  - More latency, less throughput
  - Mainly for circuit switched network
- Buffered flow control
  - Mainly for packet switched networks

Challenges

Decision & challenges [3]

- Links: serial or parallel?
- Router architecture: which routing protocol? cost-effectiveness vs. performance?
- Area: switching protocol? buffer/link sizing? topology?
- Latency: packetization, routing protocol overhead, topology?
- Power consumption: power of routing blocks, redundancy?

Implementations

Implementation

- FlexNoC [5]
- Ncore (cache coherent) [6]
- XPIPES [7]

Simulation [8]

- Regular network simulators (f.e. OMNET, Opnet, NS2)
- Dedicated NoC simulators (f.e. Java NoC Simulator, Nirgam, Noxim, etc.)
- NoC model in full system simulator (f.e. GARNET)

Current research [8]

- 3D NoC for 3D integration technology
- Power efficiency

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