SCIENCE
PASSION
TECHNOLOGY

Digital System Design

Case study of AES

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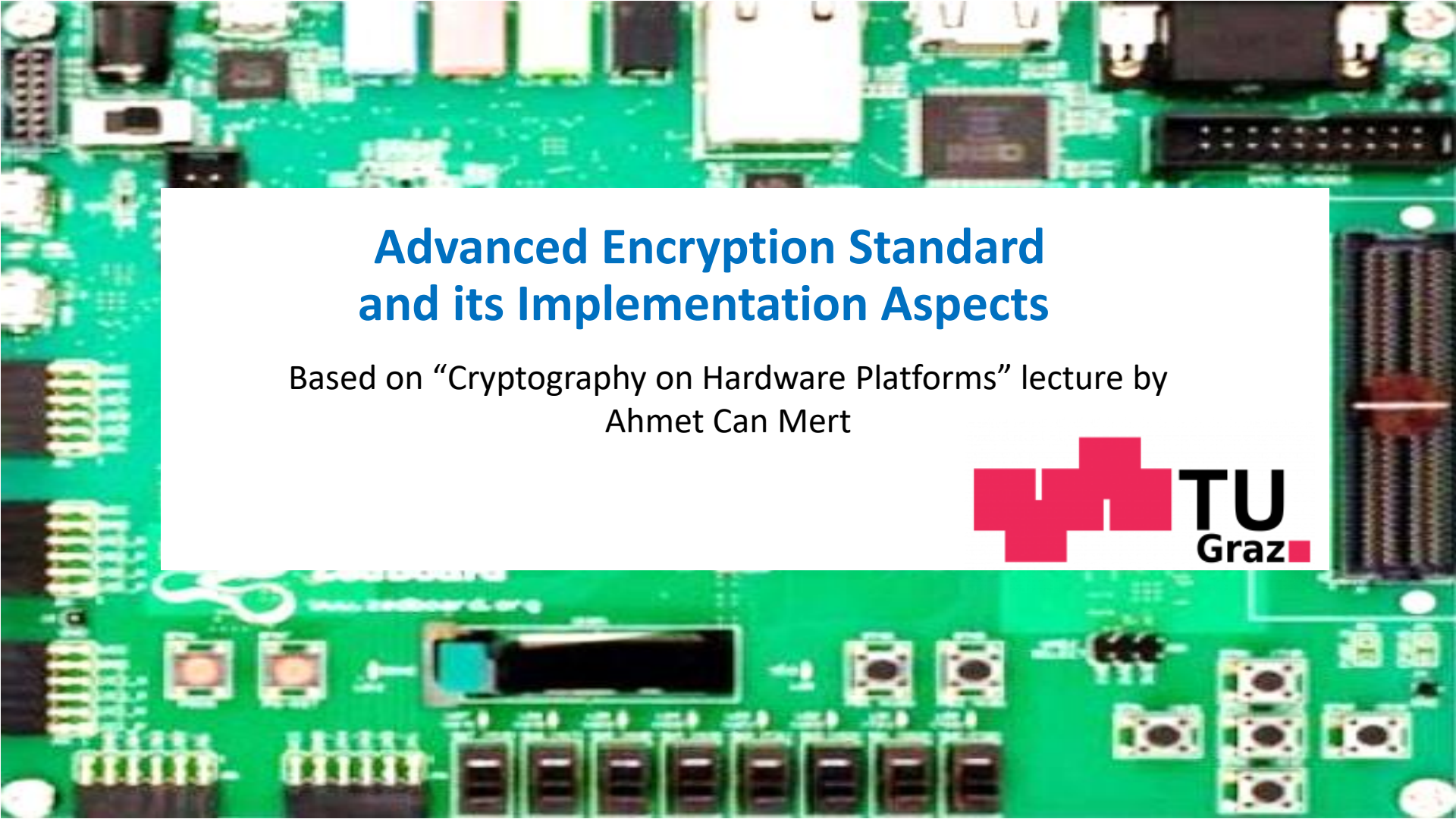
Florian Hirner
florian.hirner@iaik.tugraz.at
Graz University of Technology

https://www.iaik.tugraz.at/course/digital-system-design-705044-sommersemester-2024/

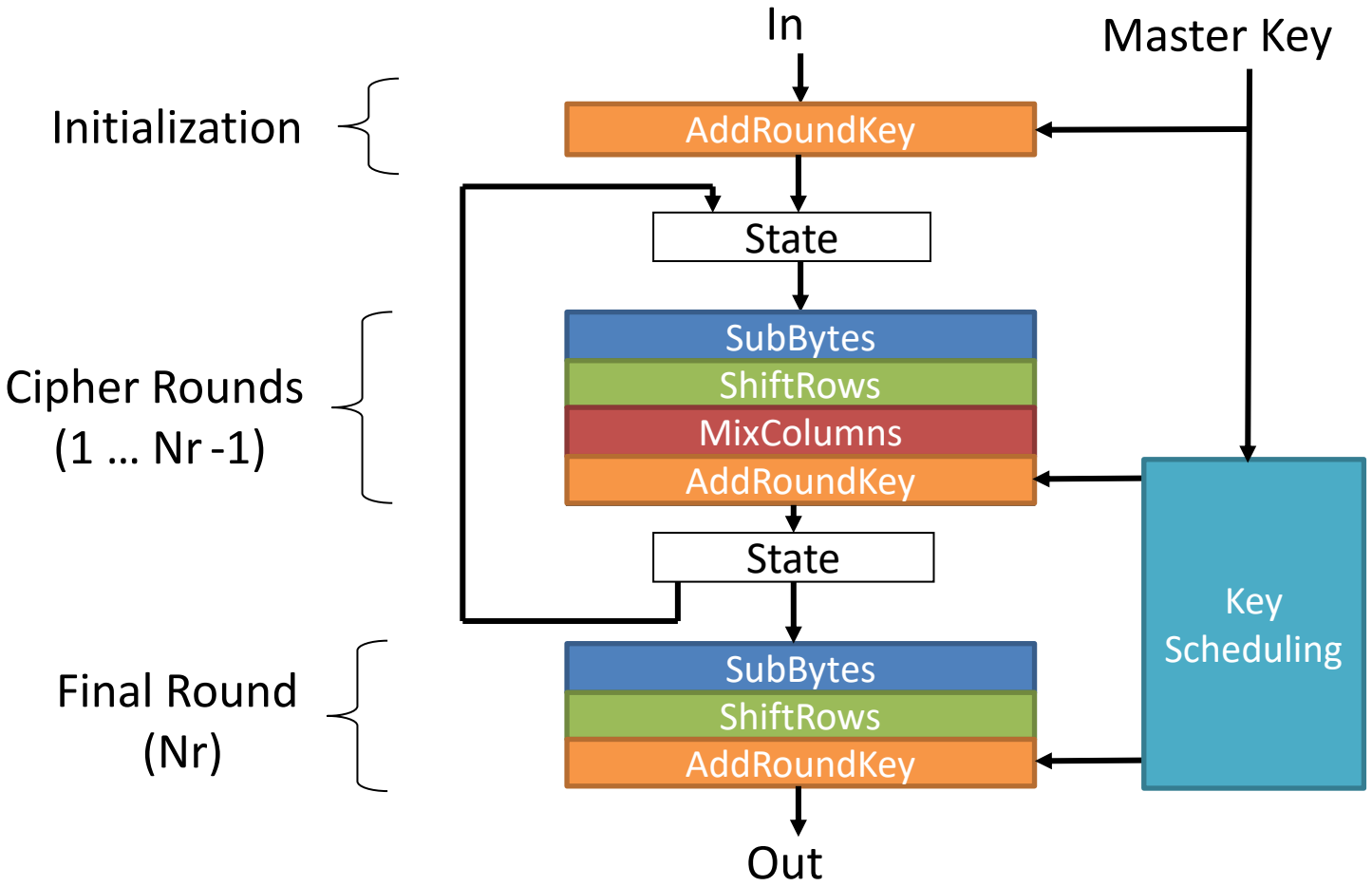


Advanced Encryption Standard and its Implementation Aspects

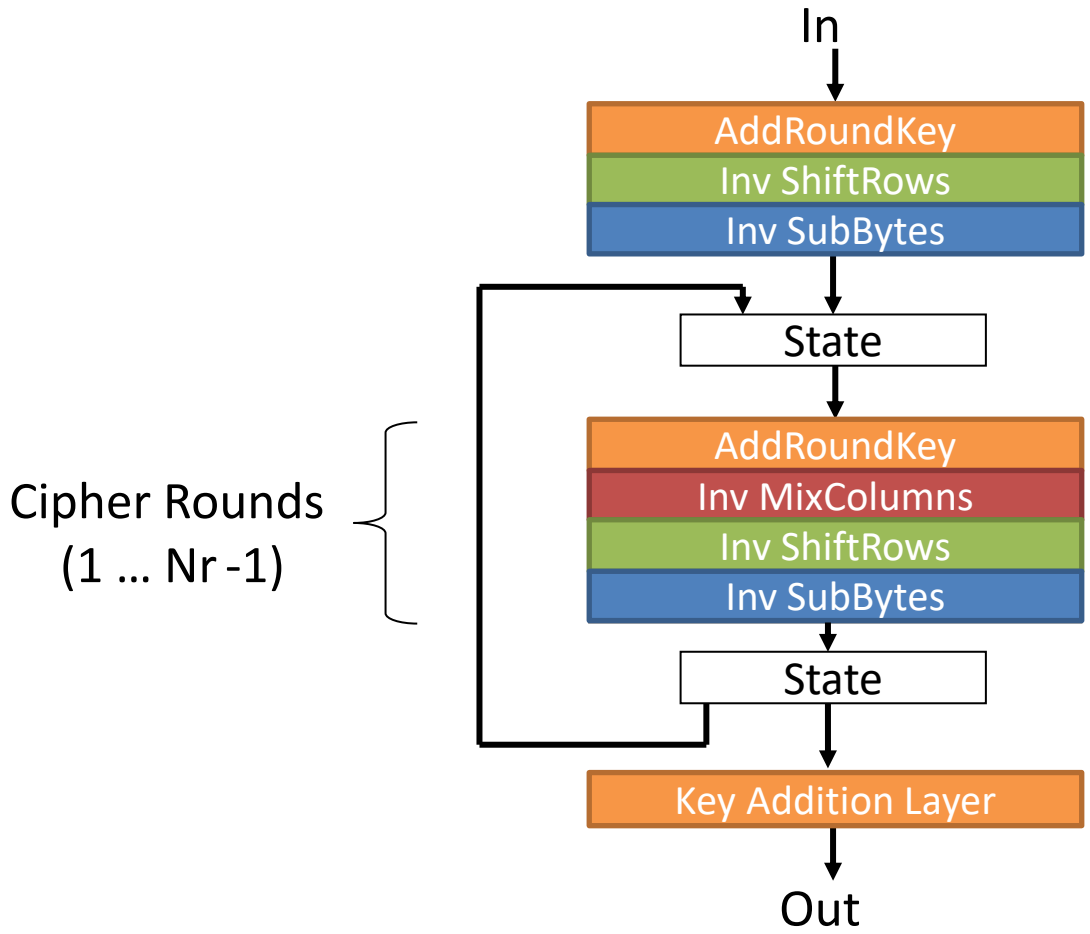
Based on “Cryptography on Hardware Platforms” lecture by Ahmet Can Mert

TU Graz

AES Encryption



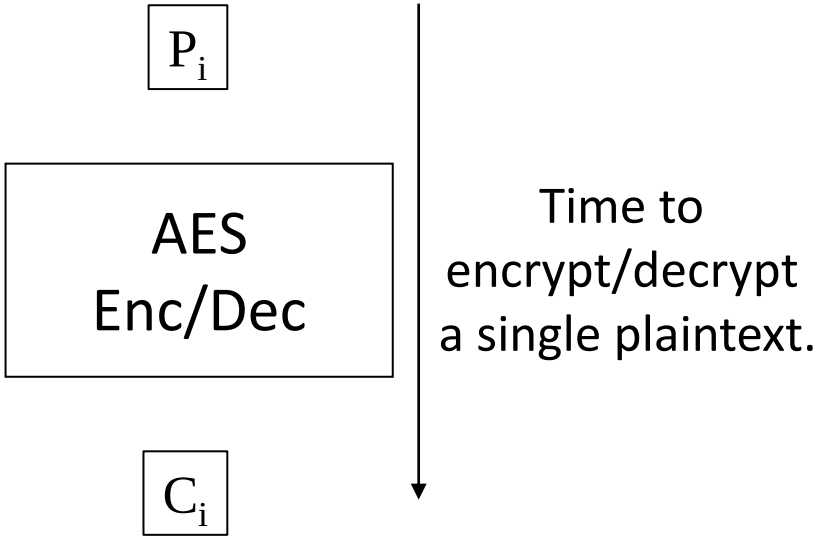
AES Decryption



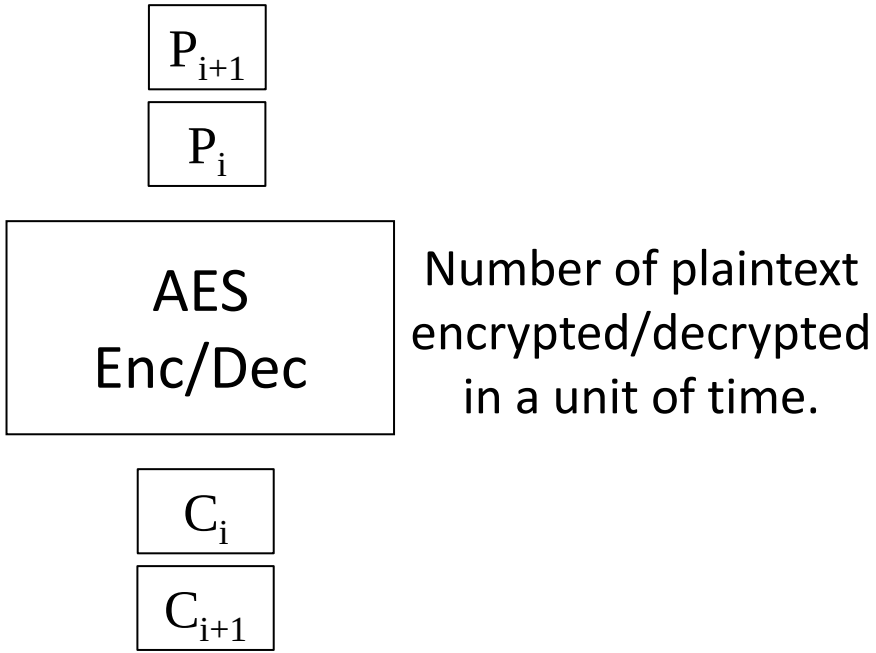
AES Implementations

- Efficiency parameters:

Latency

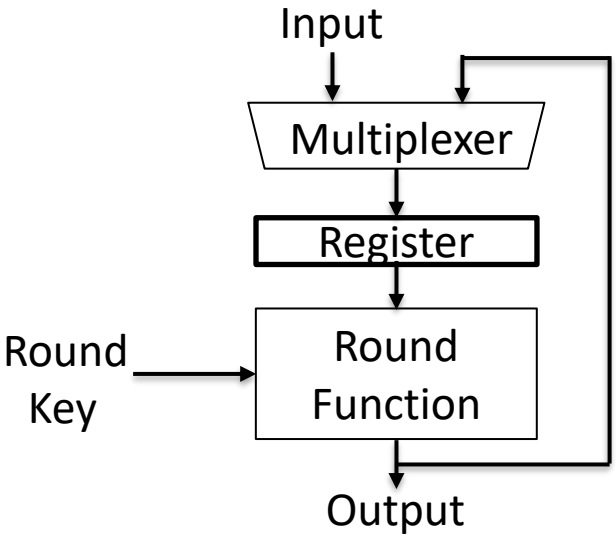


Throughput



Block Cipher Implementations: Iterative Approach

- Implement the combinational logic required for one round (supplemented with register and multiplexers). Then, use it repeatedly.
  - Only one block of data is encrypted at a time.
  - The number of clock cycles necessary to encrypt a single block of data is equal to the number of cipher rounds.



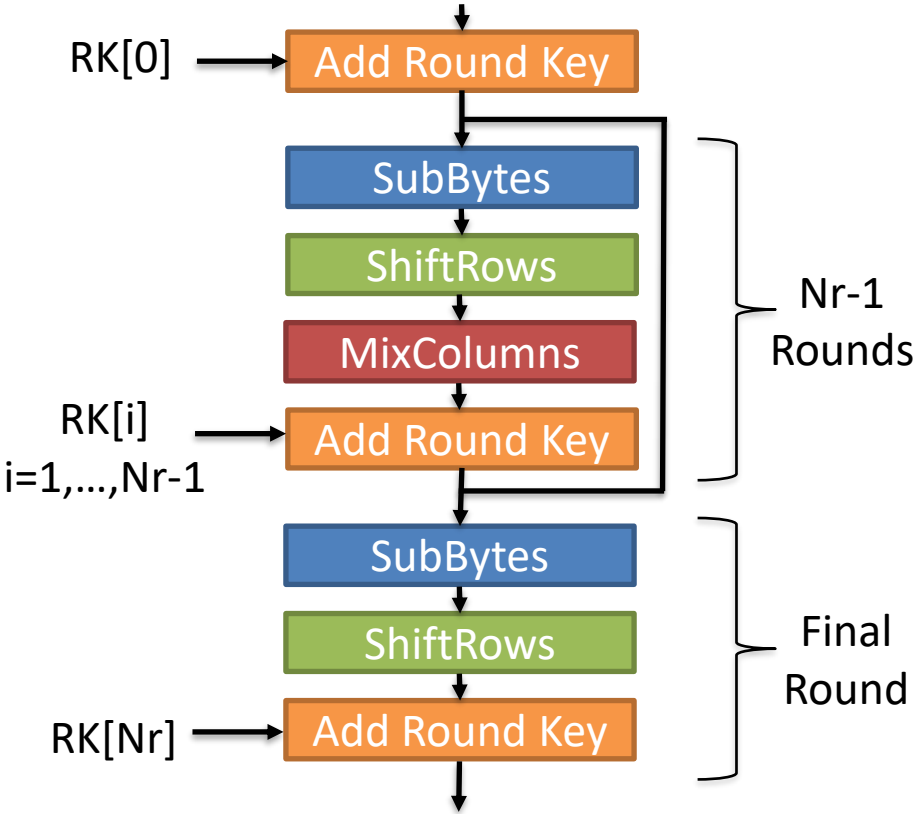
Clock period (t_{clk}) = t

Latency ≈ t *Nr

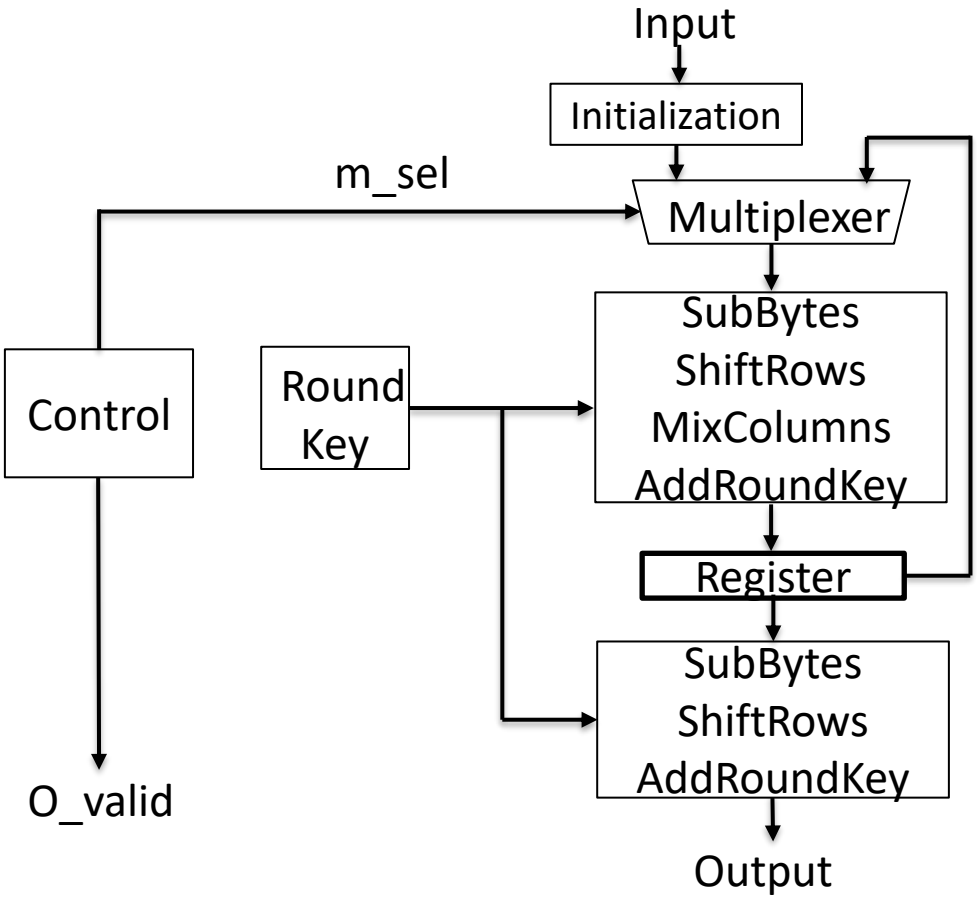
Throughput ≈ 1 / (t*Nr)

AES Implementations: Iterative Approach

- Initialization
- Round (repeated Nr-1 times):
  - SubBytes
  - ShiftRows
  - MixColumns
  - AddRoundKey
- Final Round
  - SubBytes
  - ShiftRows
  - Add Round Key



AES Implementations: Iterative Approach

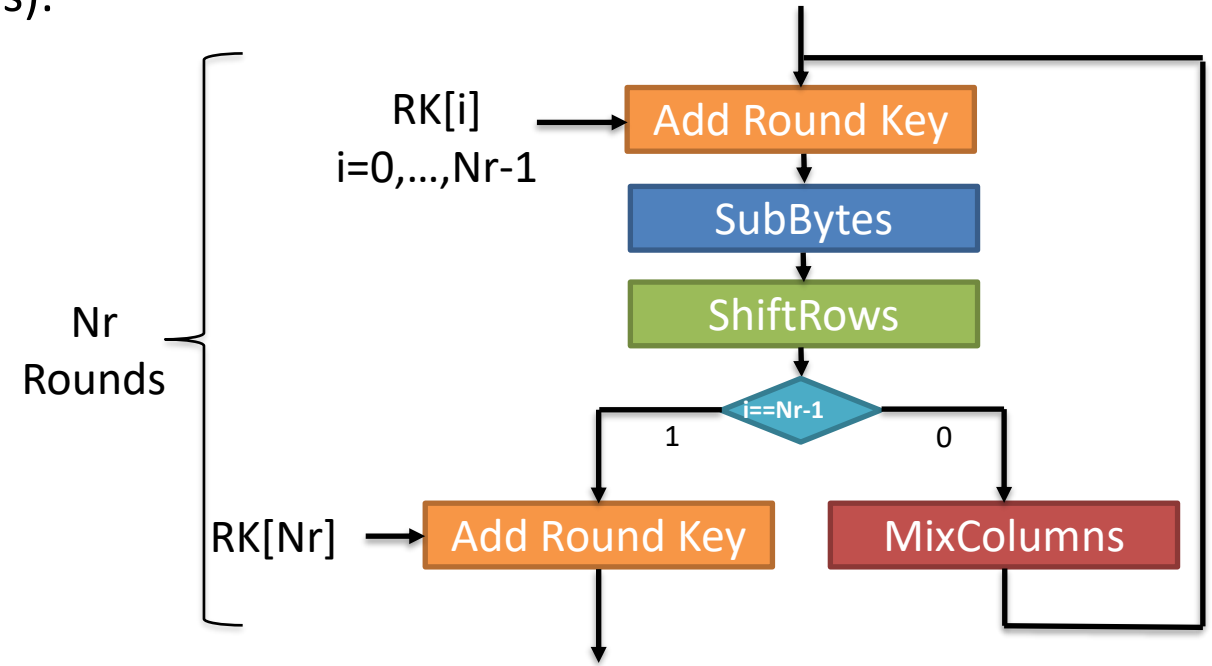


AES Implementations: Iterative Approach

- SubBytes and AddRoundKey are instantiated twice.
  - Can we do better?

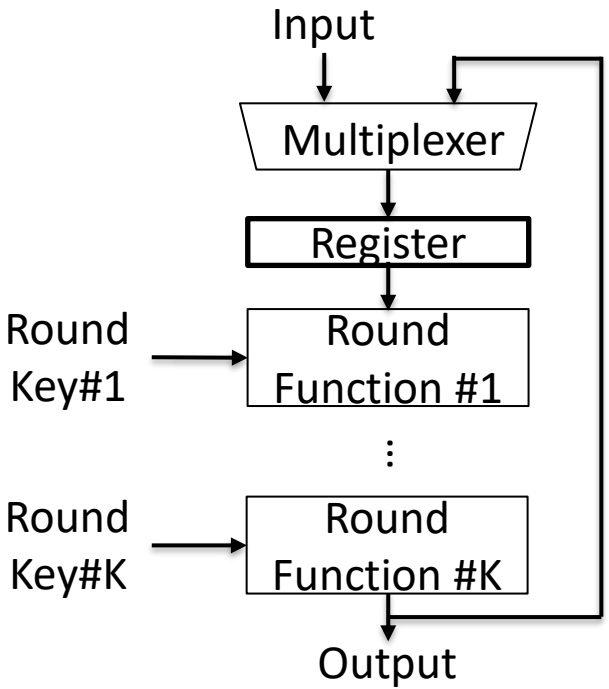
AES Implementations: Iterative Approach

- Round (repeated Nr times):
  - AddRoundKey
  - SubBytes
  - ShiftRows
  - MixColumns
    or
    AddRoundKey



Block Cipher Implementations: Partial Loop Unrolling

- *K* round out of *Nr* round functions are implemented in combinational part.
  - Partial loop unrolling.



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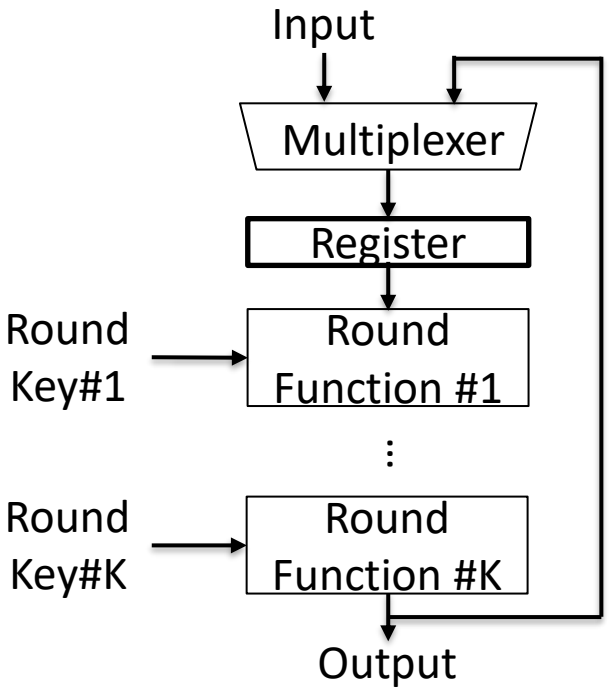


Clock period (t_{clk}) ≈ *K* . *t*

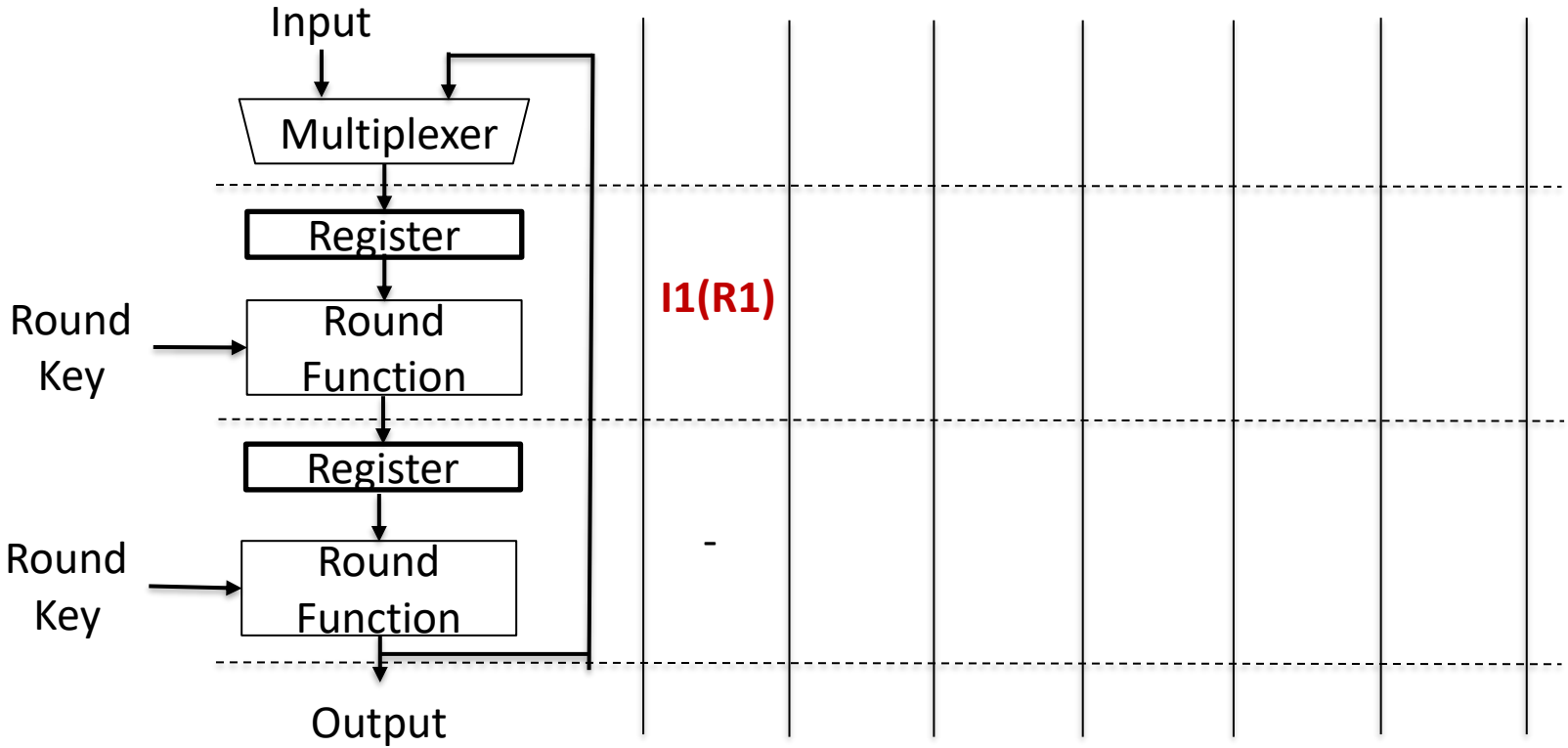
Latency ≈ *t* . (# of rounds)

Throughput ≈ 1 / (*t* . (# of rounds))

Without pipelining, unrolling offers no throughput improvement.

Block Cipher Implementations: Pipelining

- A traditional methodology for design of high-performance implementations.
  - Partial or full outer-loop pipelining (i.e., *K*=2 with *Nr*=4 rounds)



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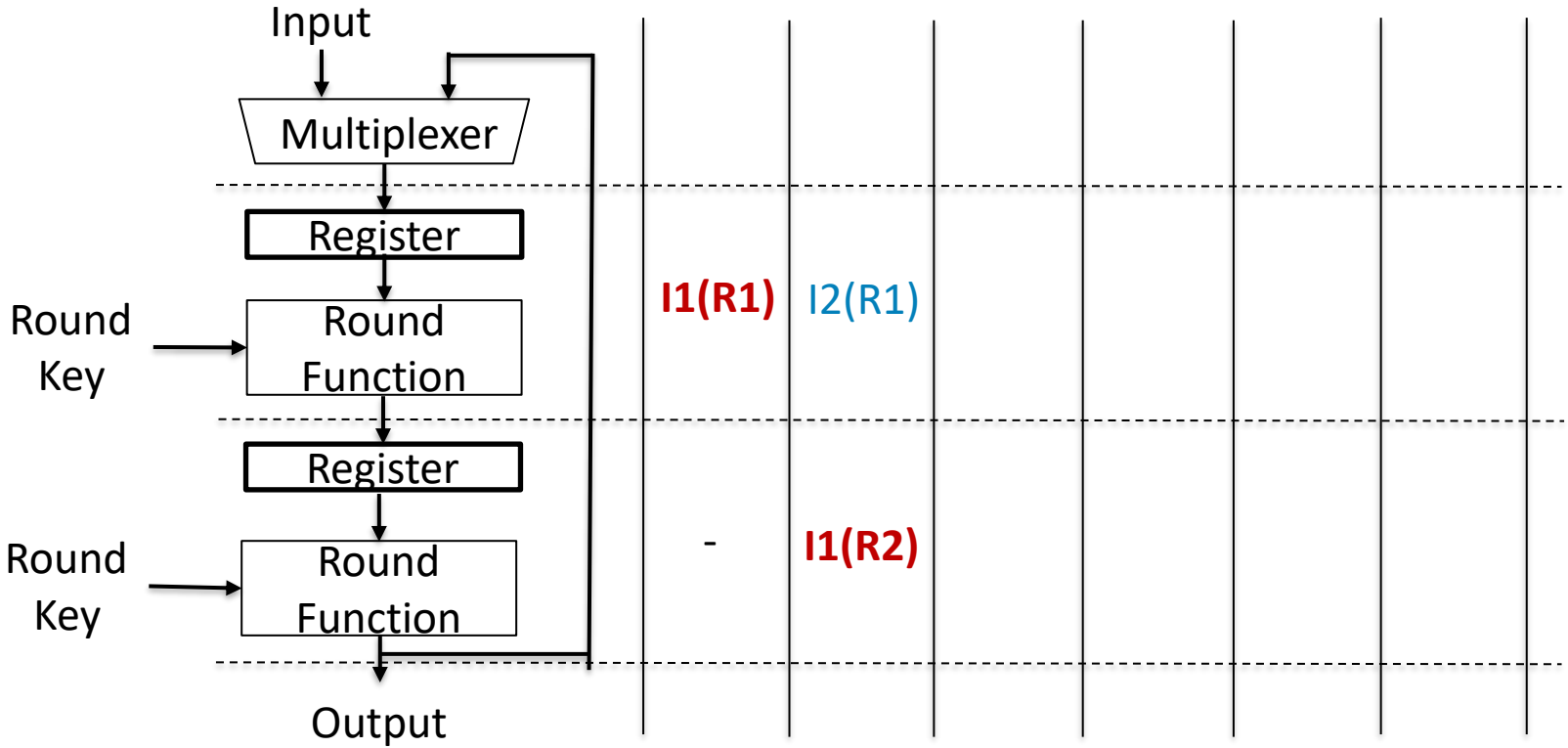

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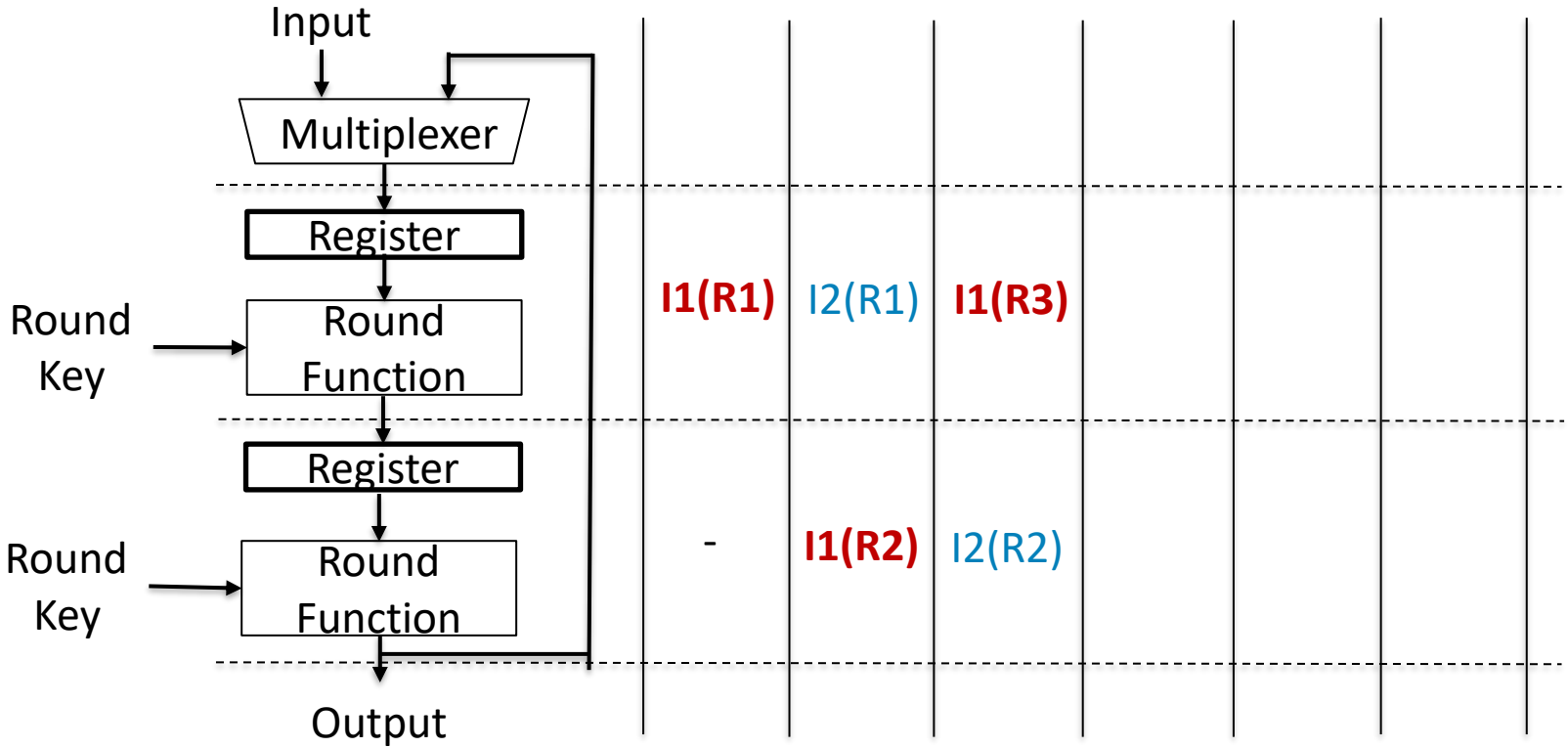

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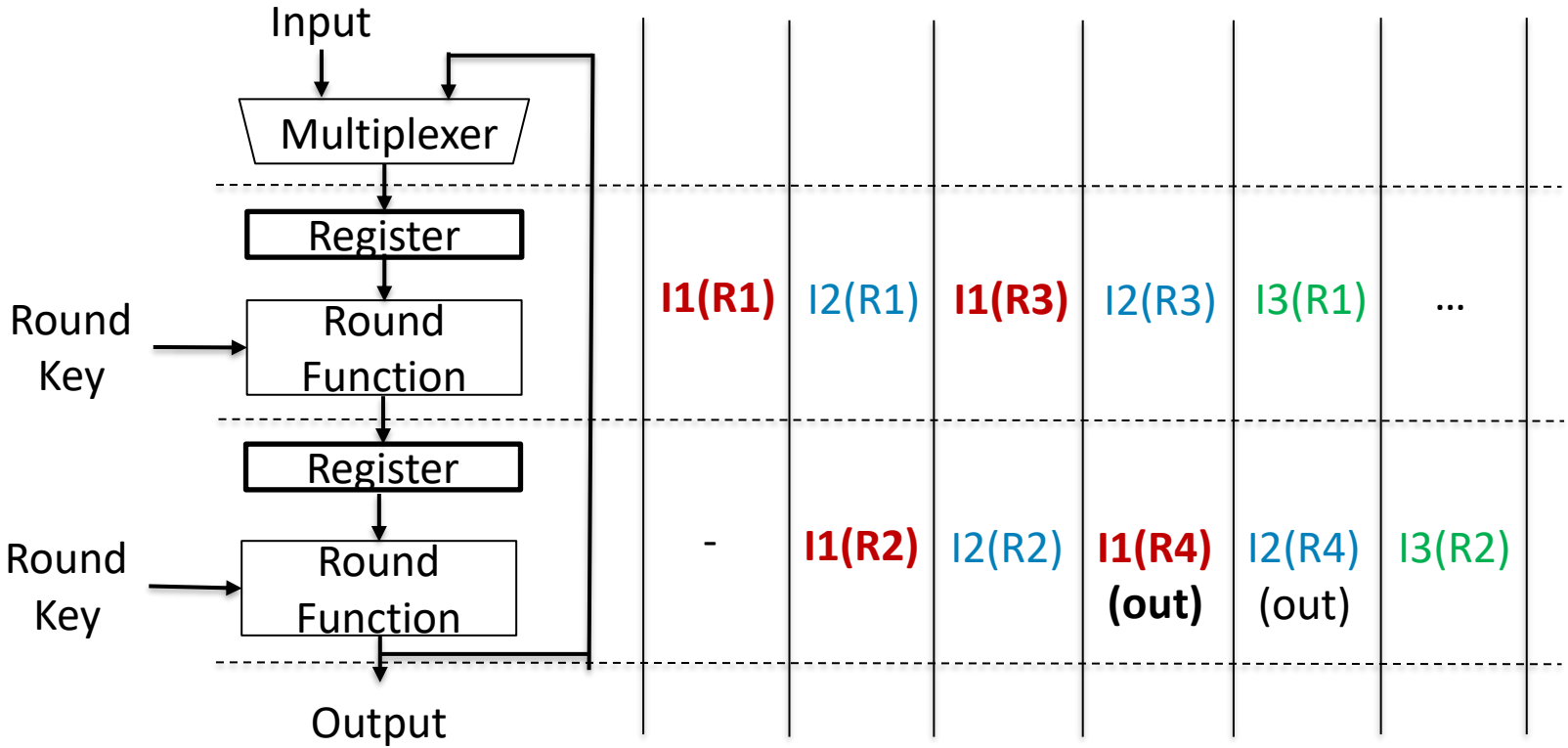
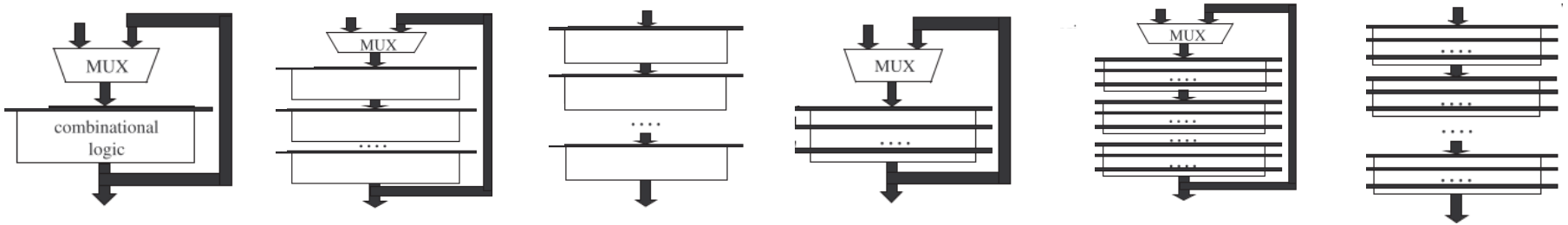


Block Cipher Implementations: Pipelining

- A traditional methodology for design of high-performance implementations.
  - Partial or full outer-loop pipelining.
  - Inner-loop pipelining.
  - Partial or full outer-loop pipelining with inner loop pipelining.

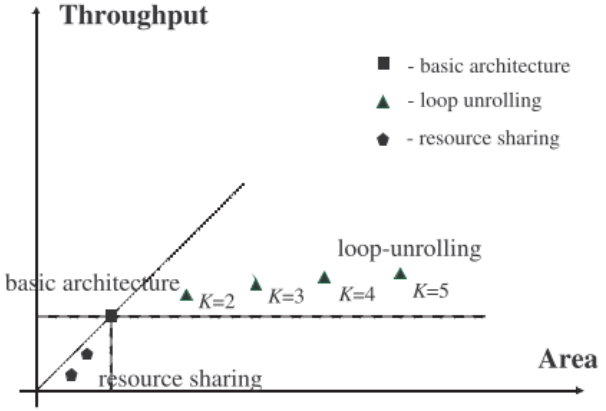


Iterative | Partial unroll | Fully unroll | Iterative with inner pipeline | Partial unroll with inner-outer pipeline | Fully unroll with inner-outer pipeline

[GC2009] K. Gaj, *FPGA and ASIC Implementations of AES*, Cryptographic Engineering, 2009.

Block Cipher Implementations: Summary

- Summary of implementation methods
  - Iterative
  - Partial unroll
  - Fully unroll



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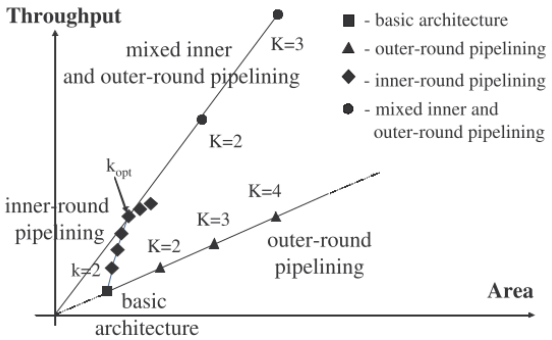
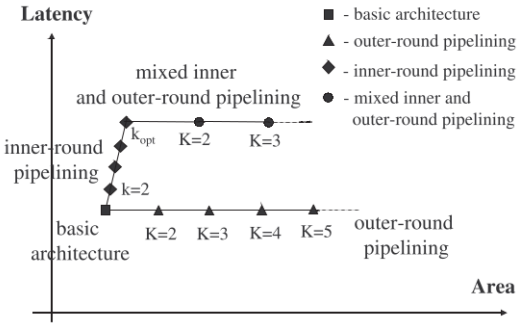
Block Cipher Implementations: Summary

- Summary of implementation methods
  - Iterative
  - Partial unroll
  - Fully unroll
  - Pipelining
    - Inner
    - Outer





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References

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[GC2009] K. Gaj, *FPGA and ASIC Implementations of AES*, Cryptographic Engineering, 2009.