TU Graz

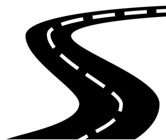
SCIENCE
PASSION
TECHNOLOGY

SoC Debugging Tutorial

Barbara Gigerl, Rishub Nagpal

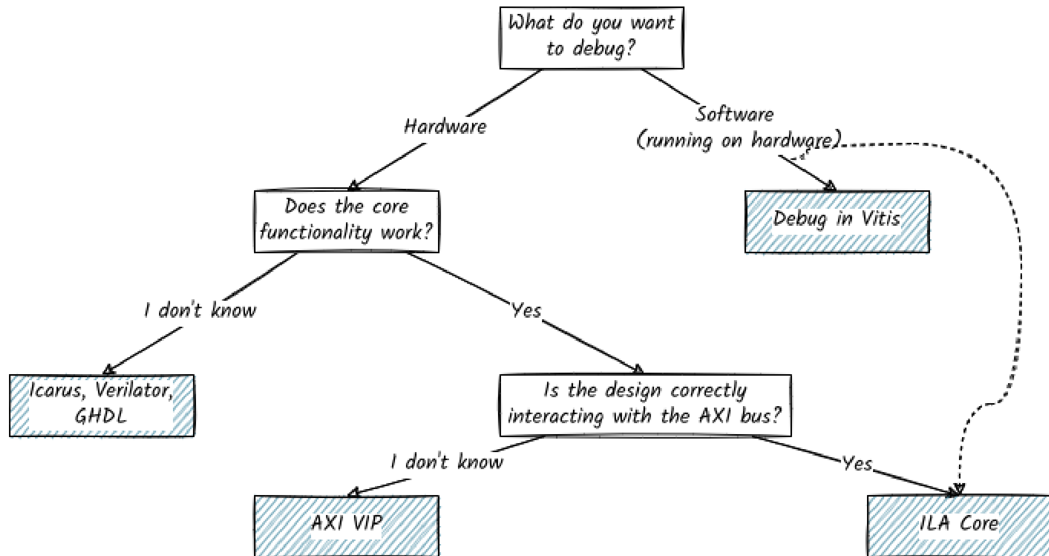
October 19th, 2022

Overview



- Simulation of hardware designs (Icarus, Verilator, GHDL)
- Using AXI VIP
- Using ILA Cores
- Debugging SW in Vitis

Can’t decide?



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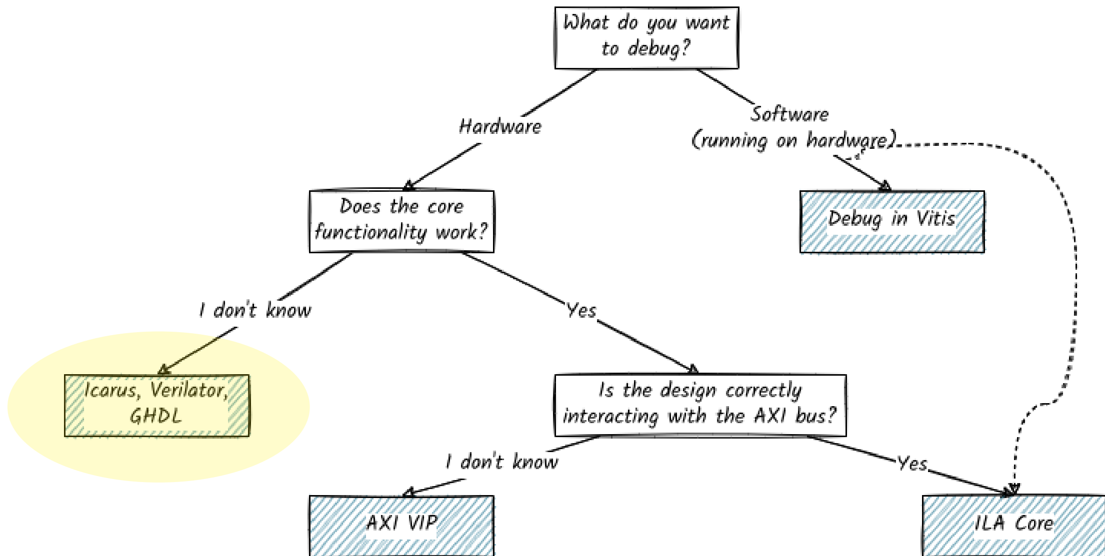

Simulation of hardware designs

Icarus, Verilator, GHDL

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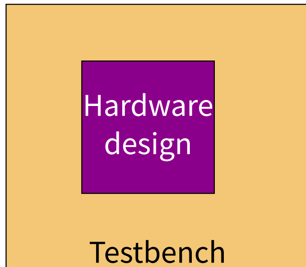

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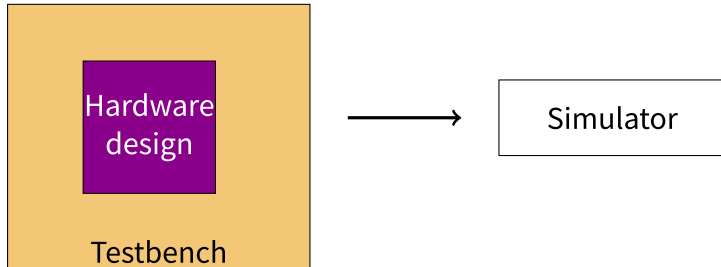

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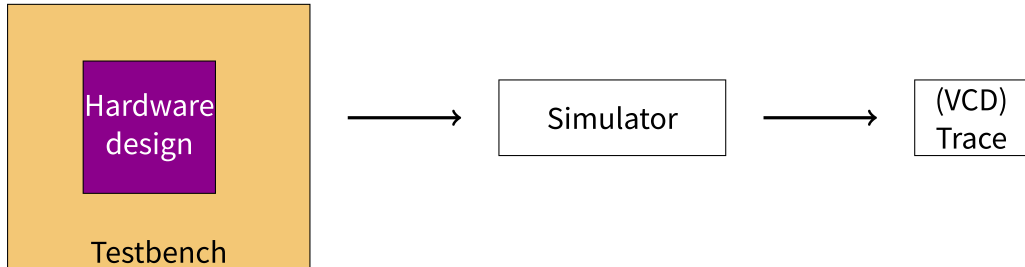

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```
iverilog -o <bin_name> <dut>.v <tb>.v
./<bin_name>
```

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```
verilator --trace --cc <dut>.v
cd obj_dir;make -f V<dut>.mk; cd ..
clang++ -Iobj_dir -I/usr/share/verilator/include verilator_tb.cpp
  obj_dir/V<dut>__ALL.a
  /usr/share/verilator/include/verilated.cpp
  /usr/share/verilator/include/verilated_vcd_c.cpp
  -o <bin_name>
./<bin_name>
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GHDL

- Simulate VHDL designs
- Testbench in VHDL
- No support for VCD

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$var wire 1 ' tx_en $end
...
$dumpvars
bxxxxxxxx #
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- Hint: Use Save Files to restore previous view configuration

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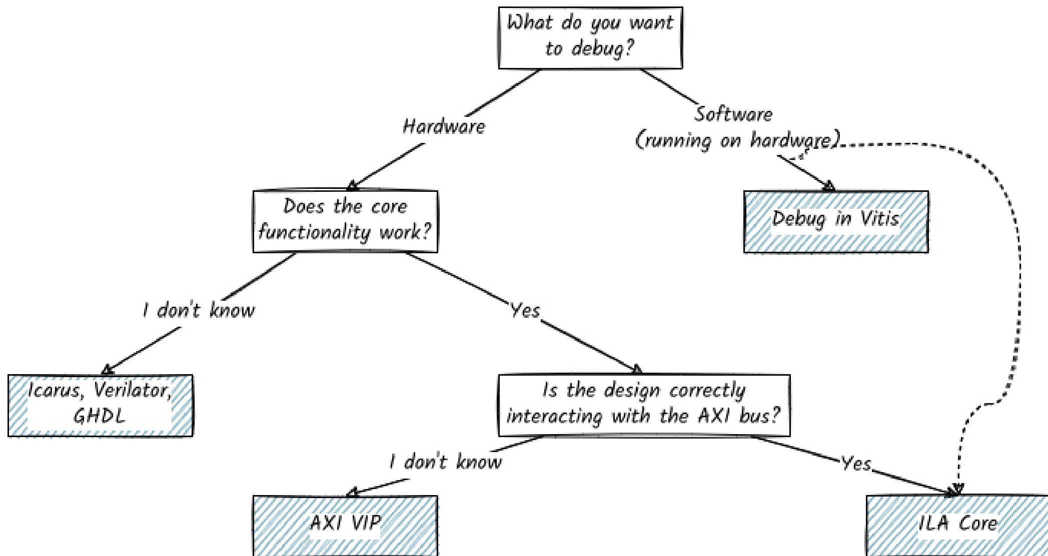

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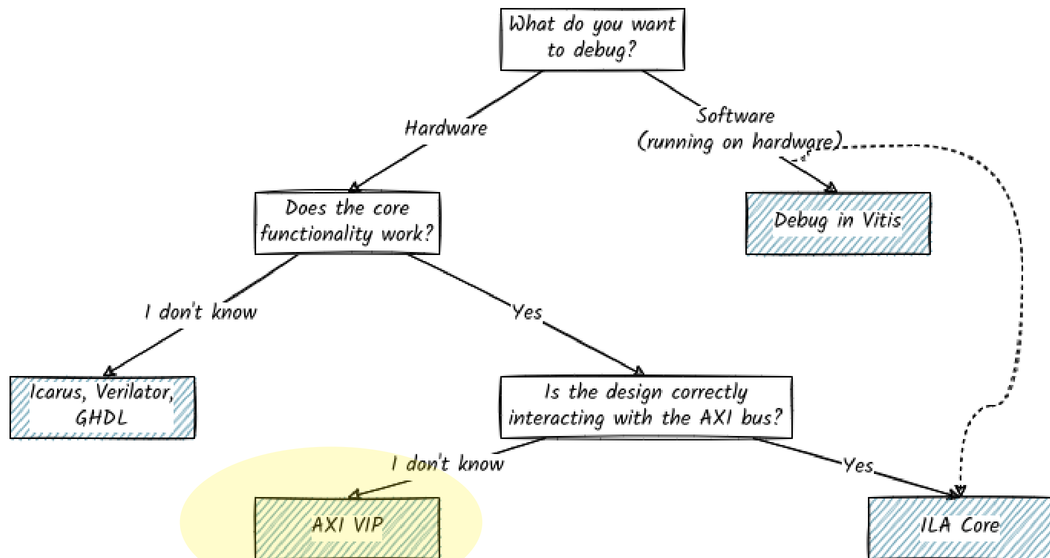

Using the AXI VIP

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- When should I use this method?
  - I want to test my IP core
    - Including AXI connectivity
    - Interaction with other IP cores on the board
    - In Vivado
  - I want to test whether my IP core reacts correctly wrt the AXI protocol

AXI crashcourse

- AXI = Advanced eXtensible Interface
- Very popular bus protocol following a master/minion[1] structure
- Masters and minions want to communicate with each other via a shared channel.
  - Master reads data from and writes data to minion.
  - Minion does nothing without command from master.
- Based on bursts

[1]= slave

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  - AXI pass-through VIP: passive monitor

Preparing the test setup

1. Create a new block design and add:
   a. The IP core you want to test (AXI minion)
   b. `AXI verification IP`
   c. `Simulation clock generator`
2. Connect the simulation clock to the DUT-IP and VIP
3. Configure VIP: `Customize block...`
   - Interface mode: Master, minion, pass-through
4. `Run connection automation...`
5. `Validate design`
6. `Create HDL wrapper`

Writing the testbench

1. Add a new simulation source (`tb.sv`)
2. Import: `import axi_vip_pkg::*;` and `import <axi_vip_name>_pkg::*;` Hint: use `get_ips *vip*` to find out name
3. Instantiate the HDL wrapper
4. Add a new AXI master agent: `<axi_vip_name>_mst_t master_agent;`
   - Master agent can be used to generate AXI transactions
   - `master_agent.AXI4LITE_WRITE_BURST(...)`
   - `master_agent.AXI4LITE_READ_BURST(...)`

We provide a template testbench:
https://extgit.iaik.tugraz.at/sip/tutorials/-/tree/master/axi_tb

Starting the simulation

- `SIMULATION - Run Simulation - Run Behavorial Simulation`
- `Objects` : Instantiated modules
- `Protocol Instances` : can be used to view AXI protocol behavior
- Drag into simulation window

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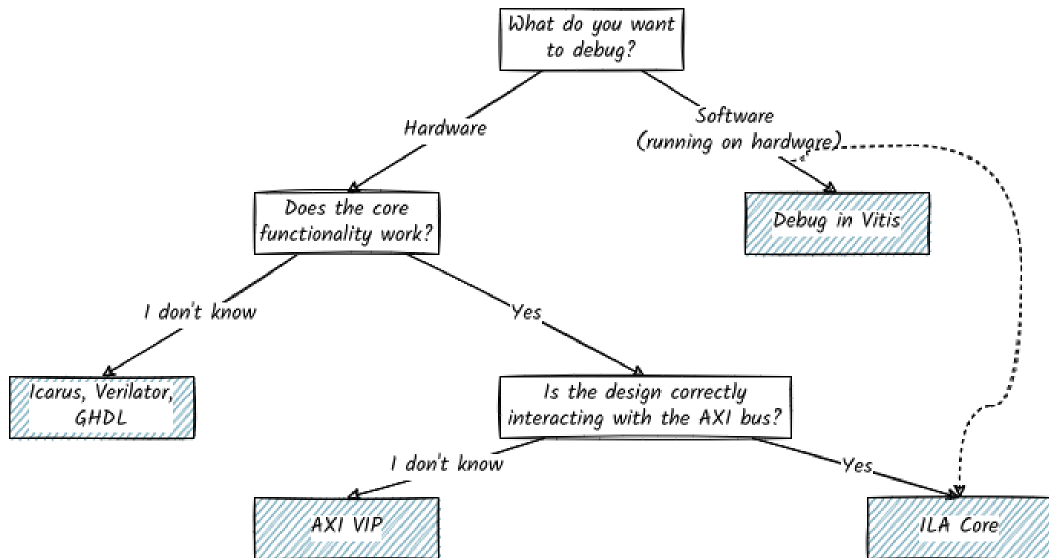

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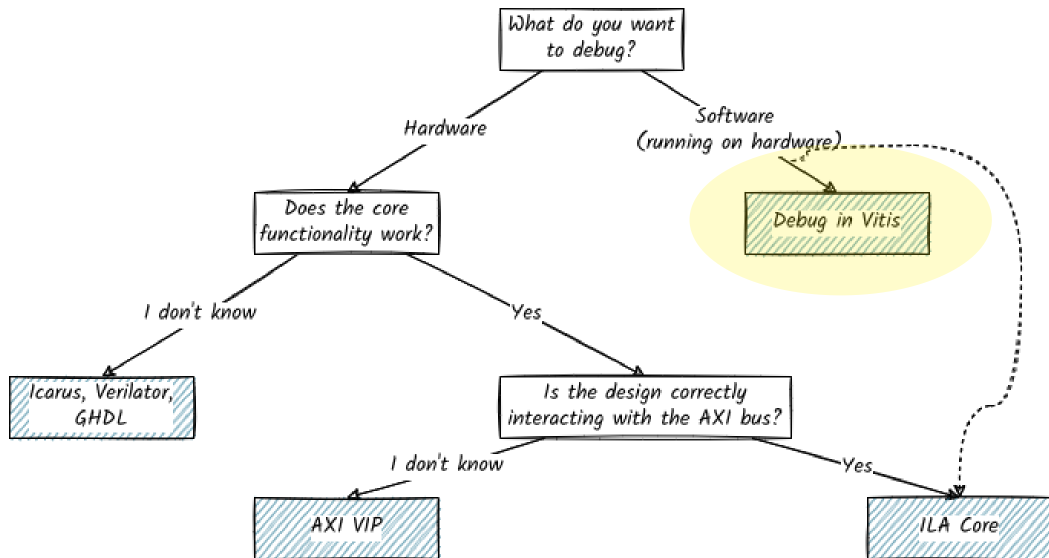

Debugging SW in Vitis

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- Executable must be built in Debug mode
  (`Assistant - Select Build Configuration`)

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- Remote debugging
  - Remote machine: runs `hw_server` from XSCT console
  - Local machine: specify hostname/IP address and port

Debugging bare-metal application in Vitis

1. Build your project
2. Connect your board via USB
3. Bare-metal applications: `Debug As - 1 Launch Hardware`
4. Connect `Vitis Serial Terminal`

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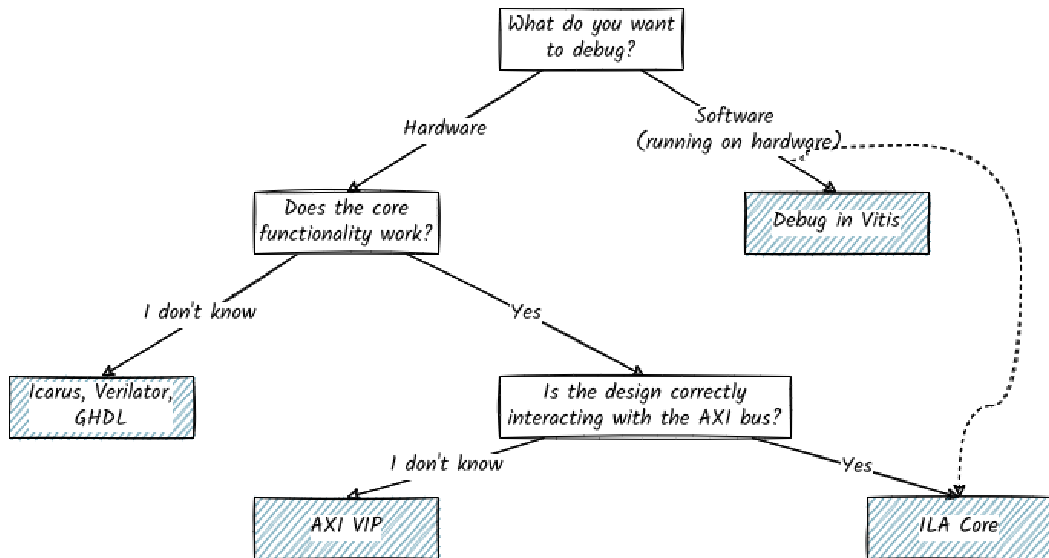

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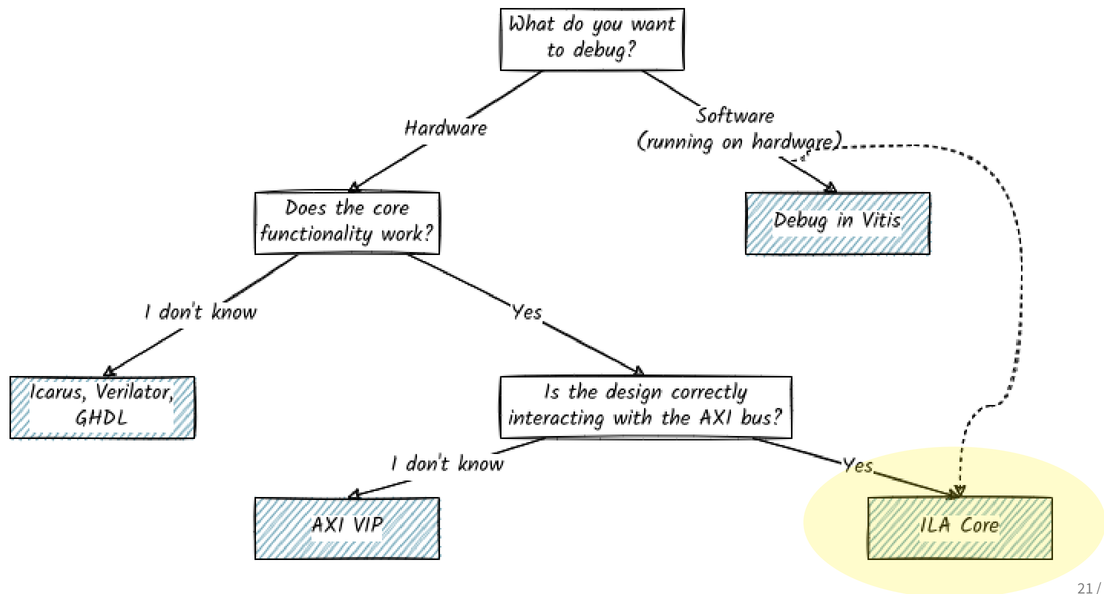

Using ILA Cores

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  - TAP can read and manipulate IO pin through logic cell

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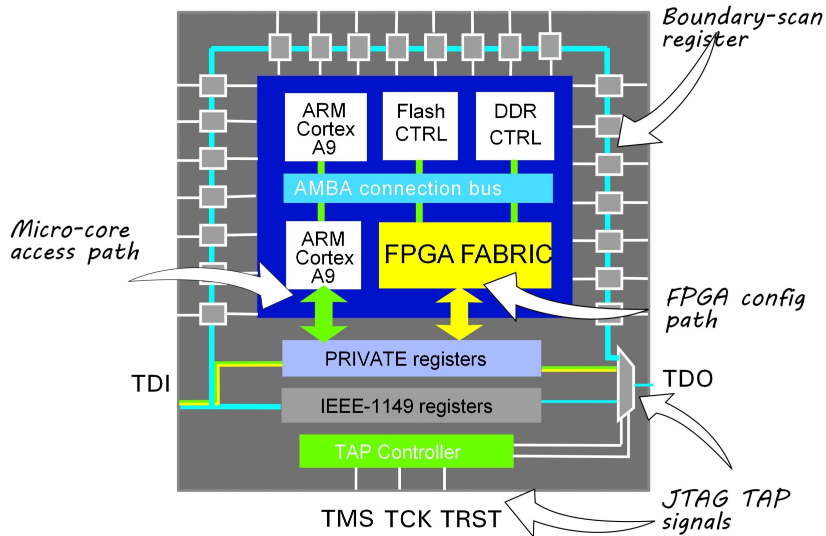

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- When should I use this method?
  - I have already verified in simulations that my hardware and software are bug free, but something still does not work out.
  - I think that synthesis/implementation introduces a bug

ILA workflow

1. In Vivado, add a new IP core to block design: `System ILA`
2. Set `Monitor Type = Native` and choose the number of probes
3. For each probe, configure the probe width and trigger.
4. Finish adding the IP and connect the ILA to the system clock.
5. For any wire to debug: select `Debug`
6. Generate bitstream and open the HW manager. Program the device (with `Bitstream file` and `Debug probes file`)
7. Run the SW in Vitis
8. In Vivado, open the HW manager and refresh target.