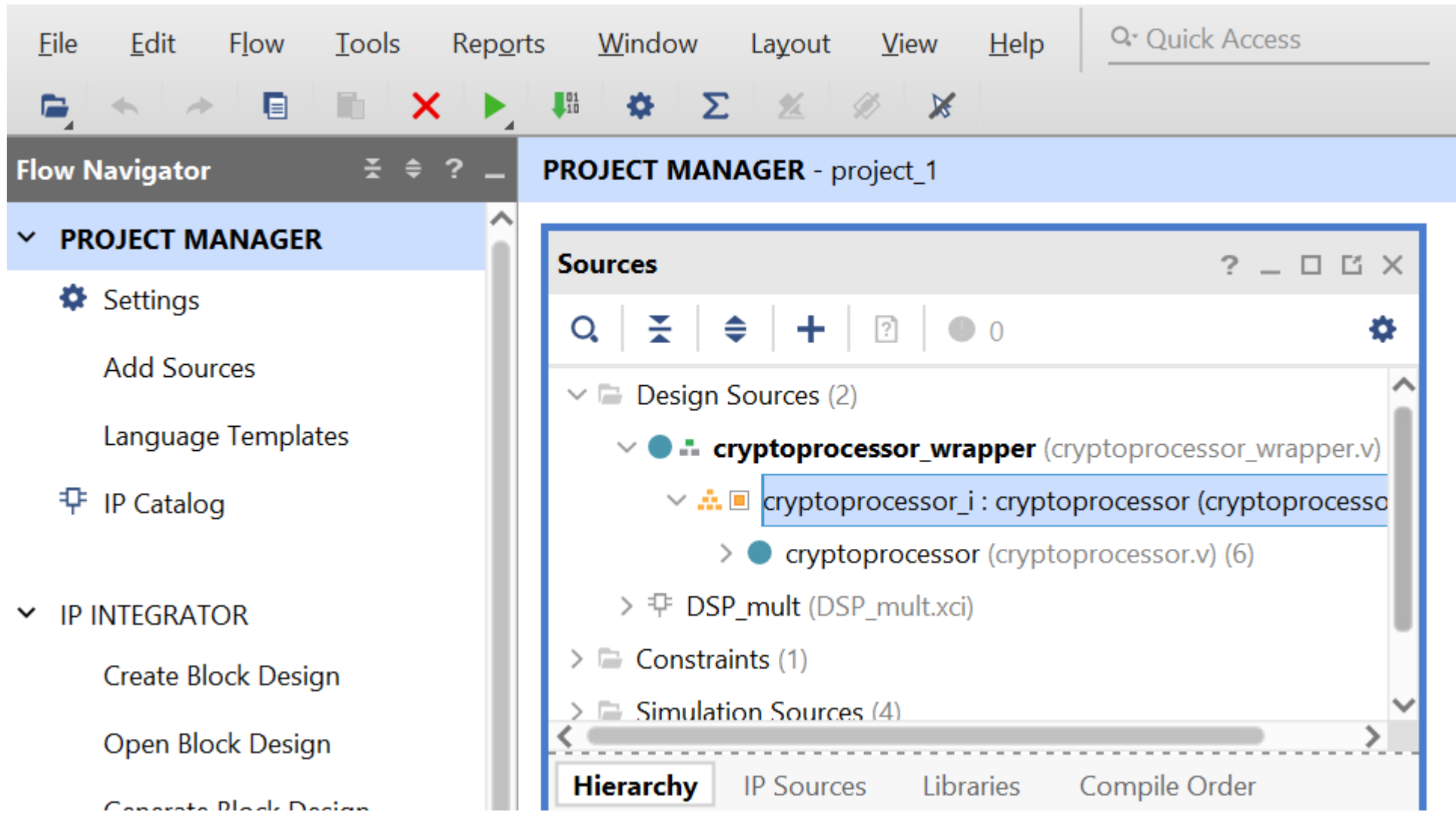


# Changing clock frequency in Vivado

**Warning: Changing the clock frequency can lead to various problems.  
Therefore, this modification is not recommended.**

Step1: Open the block diagram of the cryptoprocessor



## Step 2: Open the Zynq IP

BLOCK DESIGN - cryptoprocessor

Sources Design × Signals Board ? \_ □ ▢



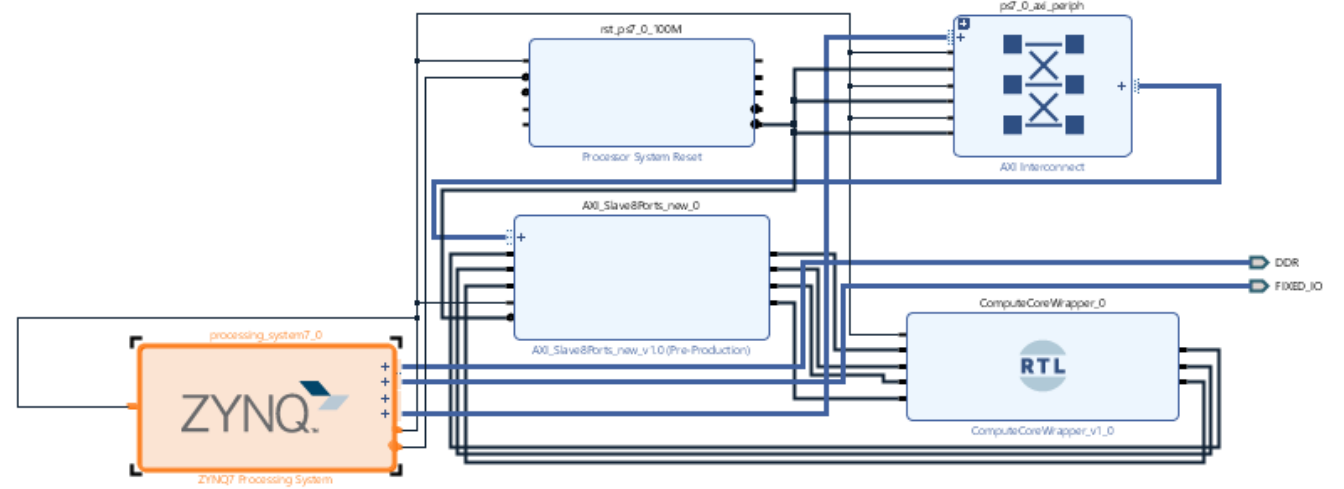
- > AXI\_Slave8Ports\_new\_0 (AXI\_Slave8Ports\_new\_v1.0:1.0)
- > ComputeCoreWrapper\_0 (ComputeCoreWrapper\_v1\_0:1.0)
- > **processing\_system7\_0 (ZYNQ7 Processing System:5.5)**

Block Properties

processing\_system7\_0

General Properties IP

Diagram × Address Editor × ? \_ □ ▢



Tcl Console × Messages Log Reports Design Runs ? \_ □ ▢

### Step3: Change the PL Fabric Clock frequency in FCLK\_CLK0

Re-customize IP

## ZYNQ7 Processing System (5.5)

Documentation Presets IP Location Import XPS Settings

Page Navigator

- Zynq Block Design
- PS-PL Configuration
- Peripheral I/O Pins
- MIO Configuration
- Clock Configuration**
- DDR Configuration
- SMC Timing Calculat
- Interrupts

Clock Configuration [Summary Report](#)

**Basic Clocking** | **Advanced Clocking**

Input Frequency (MHz) 50 CPU Clock Ratio 6:2:1

Search: Q-

Component	Clock S...	Requested...	Actual Fre...	Range(MHz)
> Processor/Memory Clocks				
> IO Peripheral Clocks				
▼ PL Fabric Clocks				
<input checked="" type="checkbox"/> FCLK_CLK0	ARM	100	100.000000	0.100000 : 250.00
<input type="checkbox"/> FCLK_CLK1	IO PLL	50	10.000000	0.100000 : 250.00
<input type="checkbox"/> FCLK_CLK2	IO PLL	50	10.000000	0.100000 : 250.00
<input type="checkbox"/> FCLK_CLK3	IO PLL	50	10.000000	0.100000 : 250.00
> System Debug Clocks				
> Timers				

OK Cancel

Save the change in block design and then compile the project for the new clock frequency.

The screenshot displays the Xilinx Vivado IDE interface. At the top is a menu bar with options: File, Edit, Flow, Tools, Reports, Window, Layout, View, Help, and a Quick Access search bar. Below the menu is a toolbar with various icons for file operations, navigation, and execution. The main workspace is titled "BLOCK DESIGN - cryptoprocessor \*". On the left, the "Flow Navigator" pane is open, showing a tree view with "PROJECT MANAGER" (containing Settings, Add Sources, Language Templates, and IP Catalog) and "IP INTEGRATOR" (containing Create Block Design, Open Block Design, and Generate Block Design). The main workspace contains several panels: "Sources" (with tabs for Sources, Design, Signals, and Board), "Block Properties" (showing the selected block "processing\_system7\_0" with tabs for General, Properties, and IP), and "Tcl Console" (with tabs for Messages, Log, Reports, and Design Runs). A blue L-shaped highlight is present on the right side of the workspace, encompassing the "Diagrams" pane and the right edge of the main workspace area.