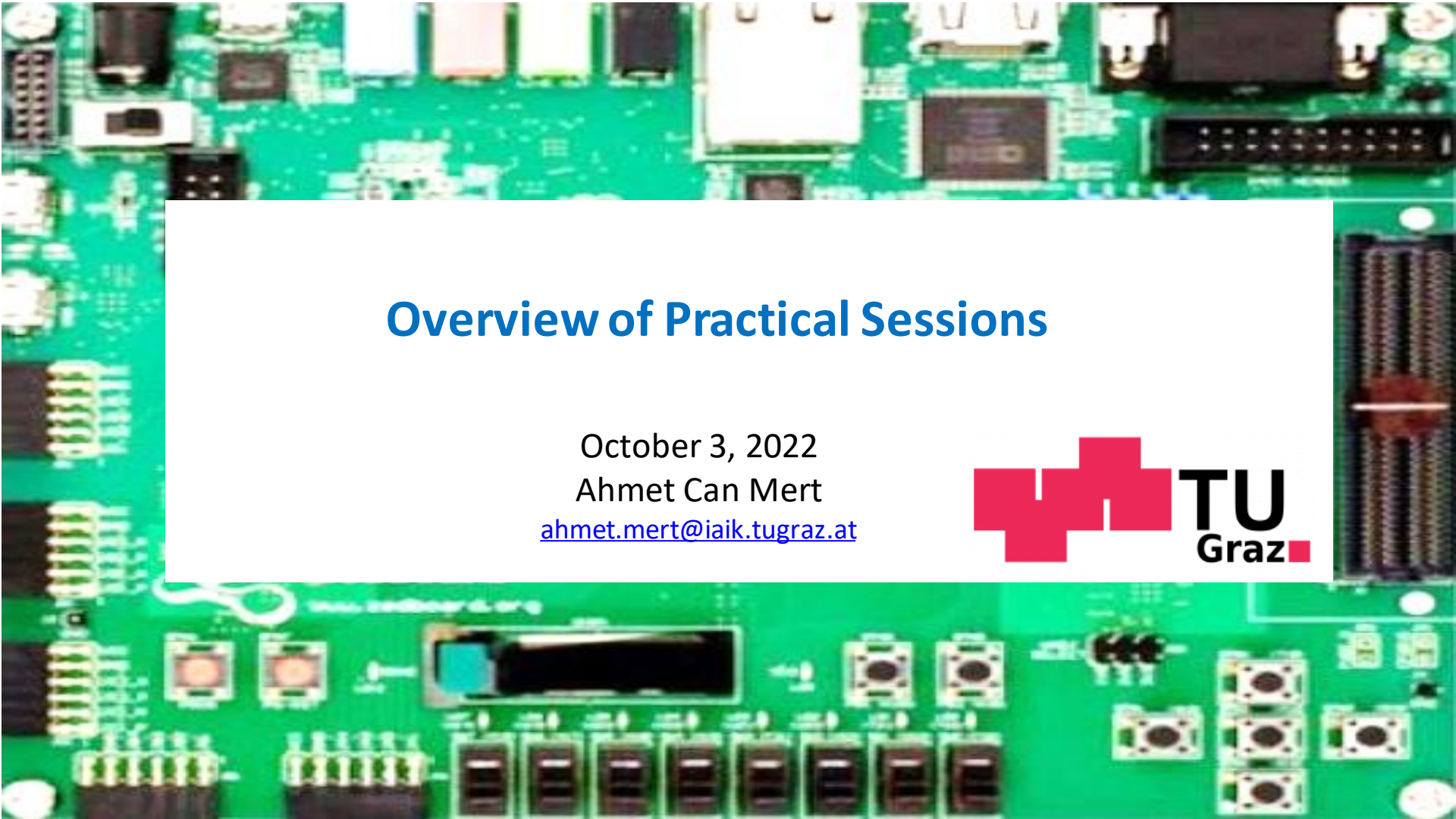

Overview of Practical Sessions

October 3, 2022

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TU Graz

A High-level Overview

- We have one hour practical session every week (Tuesday, 10:00-11:00). We will use it for ...
  - Tutorials
  - Explaining assignments
  - Office hour and Q&A

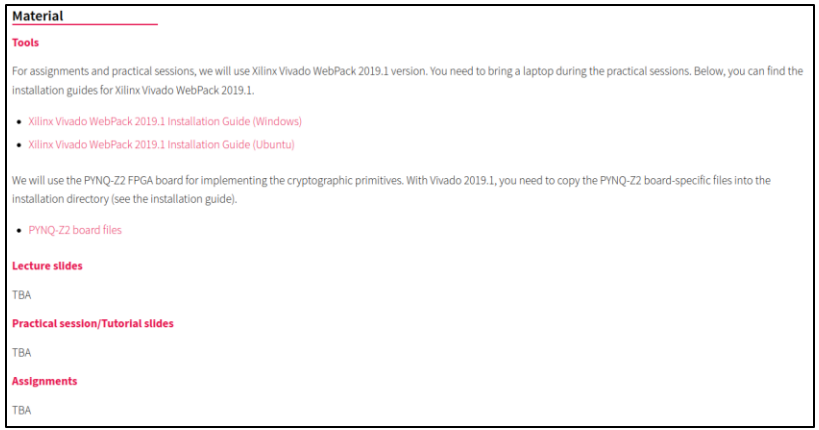
- Course webpage/Discord Channel

- Tools
  - FPGA board
  - Software
  - Coding

- Assignments

Course webpage/Discord Channel

- All course materials (lecture slides, tutorials, assignments...) will be available in course webpage.
  - https://www.iaik.tugraz.at/chw



Material

Tools

For assignments and practical sessions, we will use Xilinx Vivado WebPack 2019.1 version. You need to bring a laptop during the practical sessions. Below, you can find the installation guides for Xilinx Vivado WebPack 2019.1.

- Xilinx Vivado WebPack 2019.1 Installation Guide (Windows)
- Xilinx Vivado WebPack 2019.1 Installation Guide (Ubuntu)

We will use the PYNQ-Z2 FPGA board for implementing the cryptographic primitives. With Vivado 2019.1, you need to copy the PYNQ-Z2 board-specific files into the installation directory (see the installation guide).

- PYNQ-Z2 board files

Lecture slides

TBA

Practical session/Tutorial slides

TBA

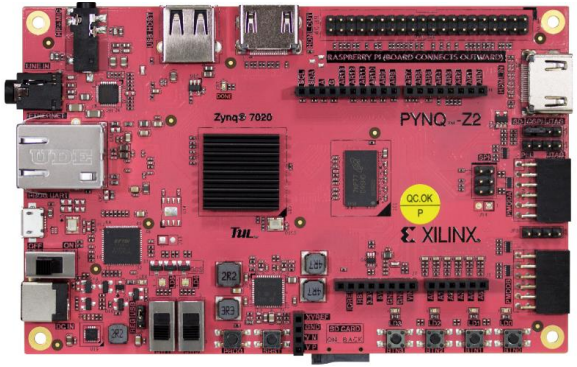
Assignments

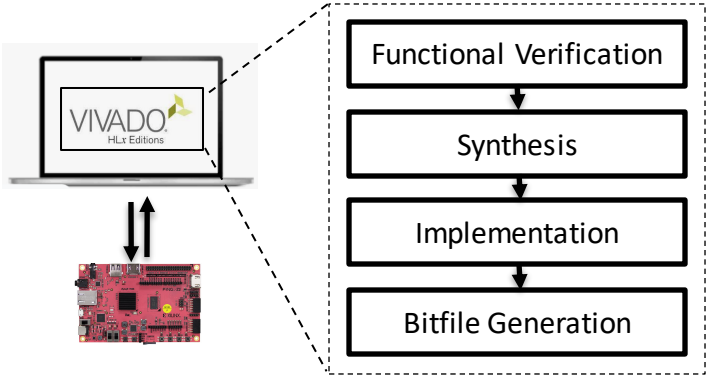
TBA

- Discord Channel
  - Announcements
  - Q&A
  - Link in the course webpage

Tools: FPGA Board

- For some parts of the assignments, we will use the PYNQ-Z2 FPGA board for implementing the cryptographic primitives.
  - Artix-7 FPGA equipped with ARM Cortex-A9 FPGA





  - Collect your board from our office (room IF02024) once you form your group
    - One FPGA per group

  - Today, we will cover FPGA basics

Tools: Software

- In the assignments, we will use Xilinx Vivado 2019.1 Webpack software for RTL simulation and FPGA programming.
  - For RTL simulation, you are free to use other tools (i.e., Modelsim).
  - We recommend Vivado.

- Installation guide in course webpage.
  - Windows and Ubuntu
  - No support for MACOS
    (We recommend Windows OS)

- For tomorrow, please bring your laptops with Xilinx Vivado 2019.1 Webpack installed.
    - Tomorrow, we will have Xilinx Vivado 2019.1 tutorial

Tools: Software

- Xilinx Vivado 2019.1 Webpack
  - Vivado for HW
  - SDK for SW

- HW/SW co-design
  - HW runs on Artix-7
  - SW runs on microprocessor

Tools: Hardware Description Languages (HDLs)

- In this course, we will use Verilog for assignments.
  - SystemVerilog is also fine
  - VHDL?

- Tomorrow, we will continue with a quick Verilog recap.

Assignments

- Two assignments
  - 100% of your grade is from assignments