Design of Mixed-Signal SoCs

Christian Zöhrer

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Outline

- Why design MS-SoCs?
- MS-SoC applications
- Analog vs. Digital
- MS-SoC design flow
- Design challenges and solutions
- MS-FPGA applications

Why design mixed-signal SoCs?

Motivation

- The real world is analog
- Continuous signals with respect to time and amplitude
- Wireless data transmission is analog
- Data processing and storage is digital
- Control units are digital (CPUs, ...)

Mixed signal - best of both worlds?

- Reduction of costs $\Rightarrow$ lower overall dye size
- Lower power consumption
- Reliability
- Performance increase:
  - EMC
  - Jitter and phase noise
  - Speed
  - SNR

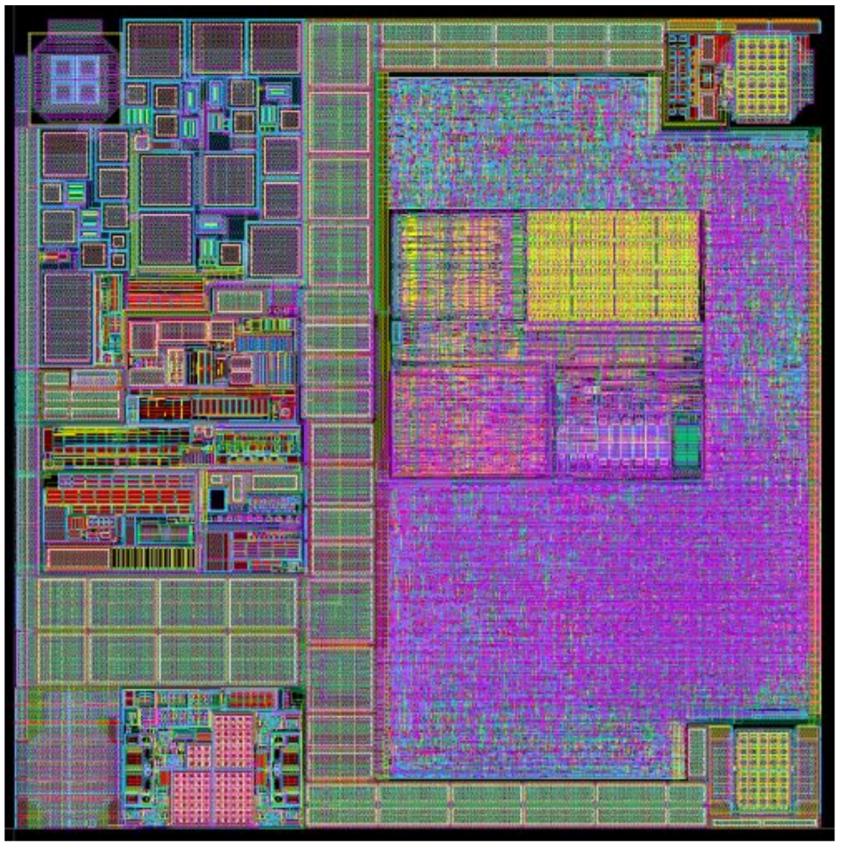

Figure 1: UHF (860MHz -960MHz) RFID passive tag IC

Applications

- Smart sensors
- Wireless communication
- Power management
- Medical devices

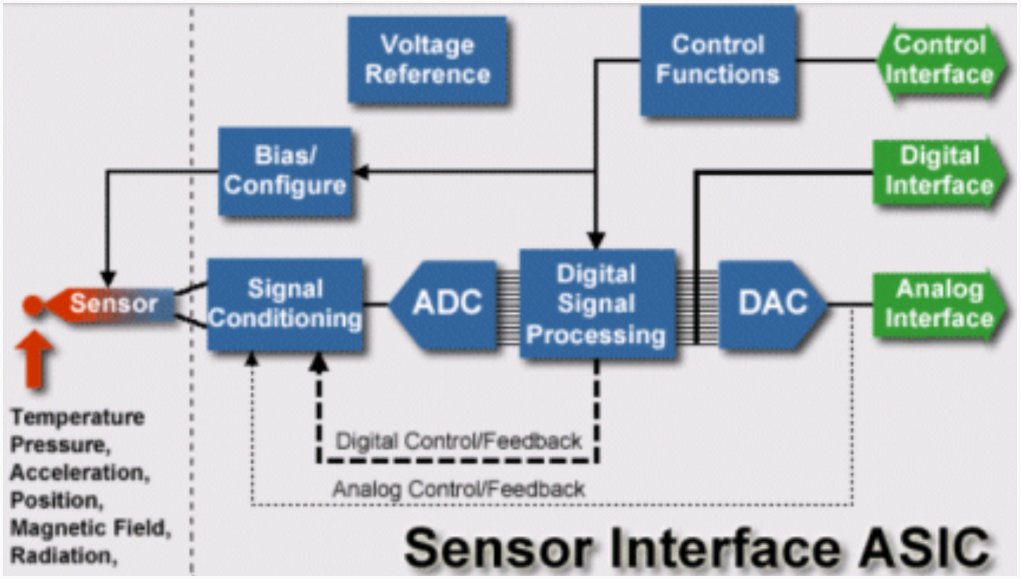

Figure 2: Smart sensor interface [**5**]

Analog vs. Digital

Analog:

- Transistor level description (netlist)
- Hand crafted layout
- Not portable (frozen IPs)
- Larger transistor size required
- Slow, high precision simulation (SPICE)

Digital:

- High-level description
- Synthesize-able
- Portable (Standard cell approach)
- Smallest transistor size possible
- Fast simulation (Verilog)

SPICE netlist

```
1 * Astable multivibrator
2 R1 N001 N002 2K
3 R2 N001 N003 2K
4 R3 N002 N004 101K
5 R4 N003 N005 100K
6 C1 N003 N004 .01u
7 C2 N005 N002 .01u
8 V1 N001 0 5
9 Q1 N003 N005 0 0 2N3904
10 Q2 N002 N004 0 0 2N3904
11 .model NPN NPN
12 .model PNP PNP
13 .lib C:\Users\...\standard.
       bjt
14 .tran 25m startup
15 .backanno
16 .end
```

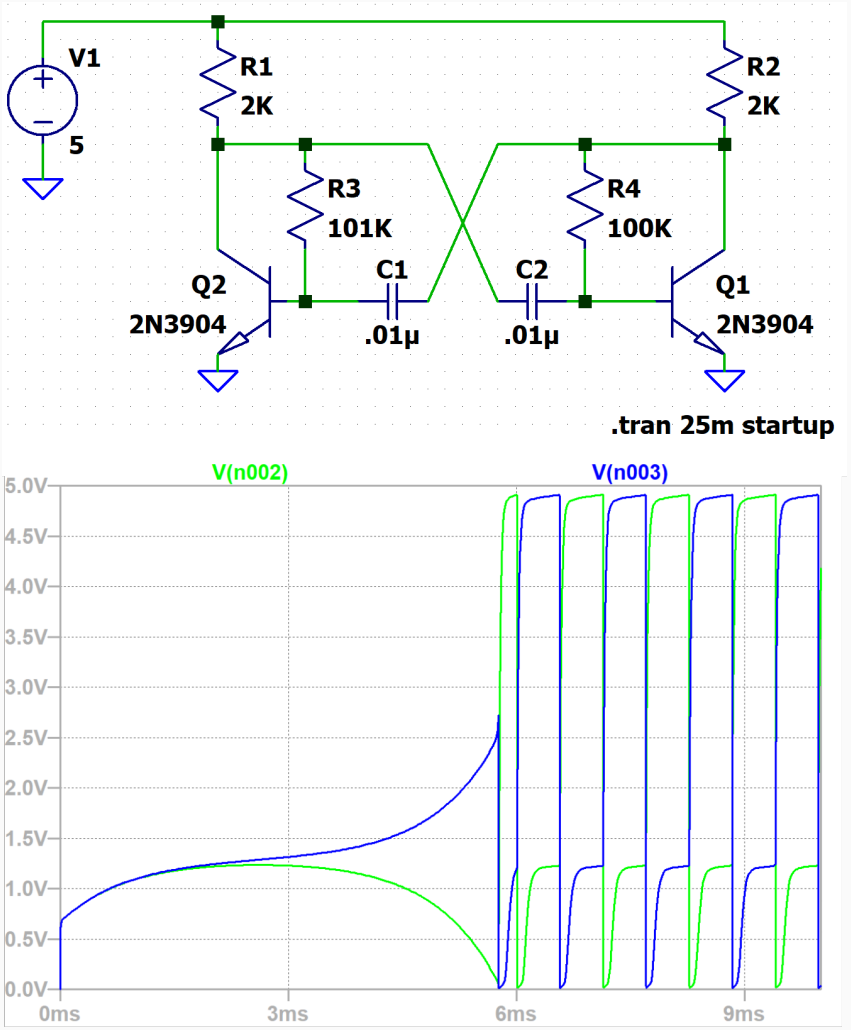

Figure 3: LT-Spice simulation

Analog vs. Digital cont.

- Technology and supply voltage are typically scaled for digital
  - Higher transit frequency f_T - higher speed of transistors
  - Reduces intrinsic gain of analog transistors
  - Smaller signal swing due to smaller voltage headroom
- Digital switching noise affects analog behavior over substrate coupling
- Difficult chip verification
- Complexity of design increases

MS-SoCs Advantages vs. Disadvantages

Advantages:

- Reduction in cost
- Performance increase
- Reliability

Disadvantages:

- Technology trade-offs
- Complex design
- Validation difficult

MS-SoC Design

Finding the right technology

- Problem of technology divergence
- Finding the *optimal* technology for analog and digital
- Digitally assisted analog
- SiP (system in package) vs. SoC
- Mixed signal FPGA applications

MS-SoC Design

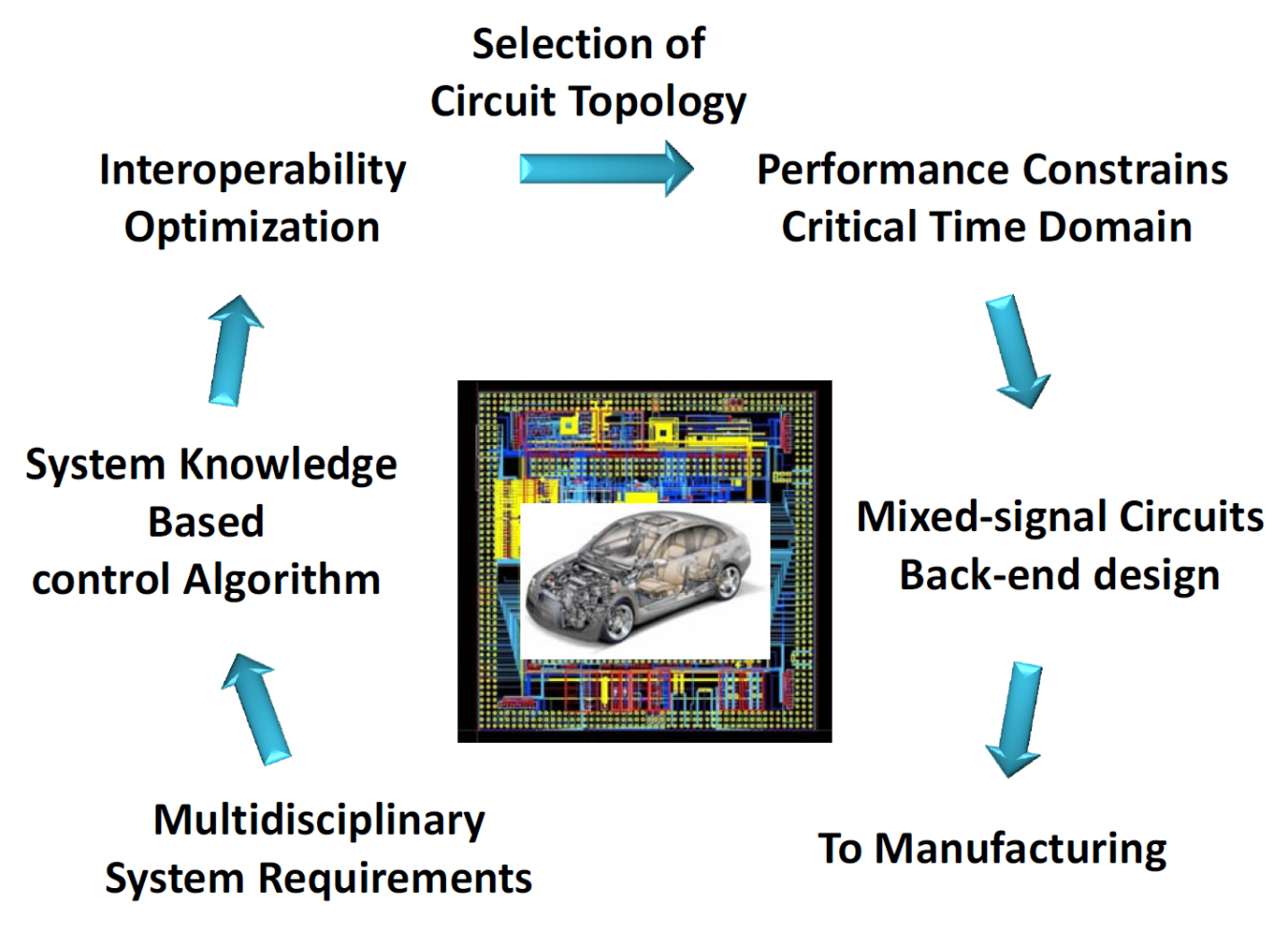

Figure 4: Collaborative design approach for MS-SoCs [4]

MS-SoC Design

- Digital design is automated:
  - Compiling high level design (standard cell methodology)
  - Floor-planning (placing macros)
  - Power routing
  - Placement
  - Clock tree synthesis
  - Routing
  - Validation (Slack)
- Analog design is implemented by hand:
  - Bottom-up design
  - Design individual blocks on transistor level
  - Validate performance vs. specification
  - Build hierarchical design by combining blocks
  - No top level simulation possible

Design flow using Black-boxing

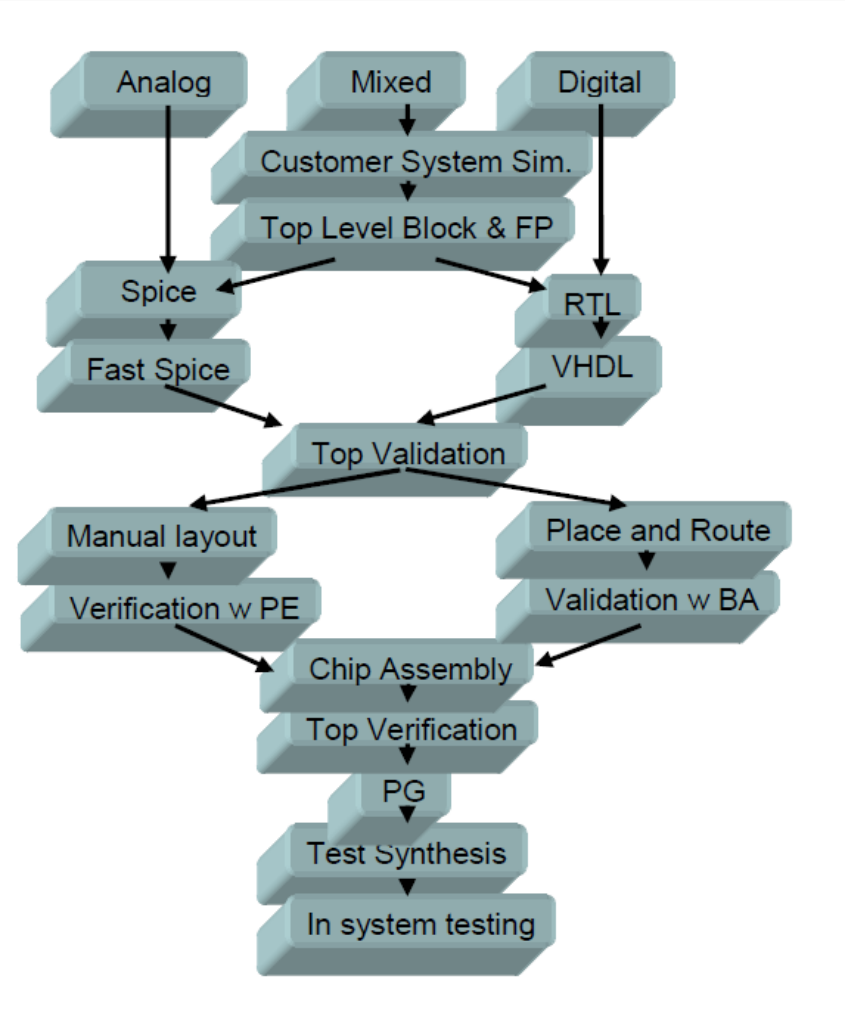

Figure 5: MS-design flow [3]

Validation problems?

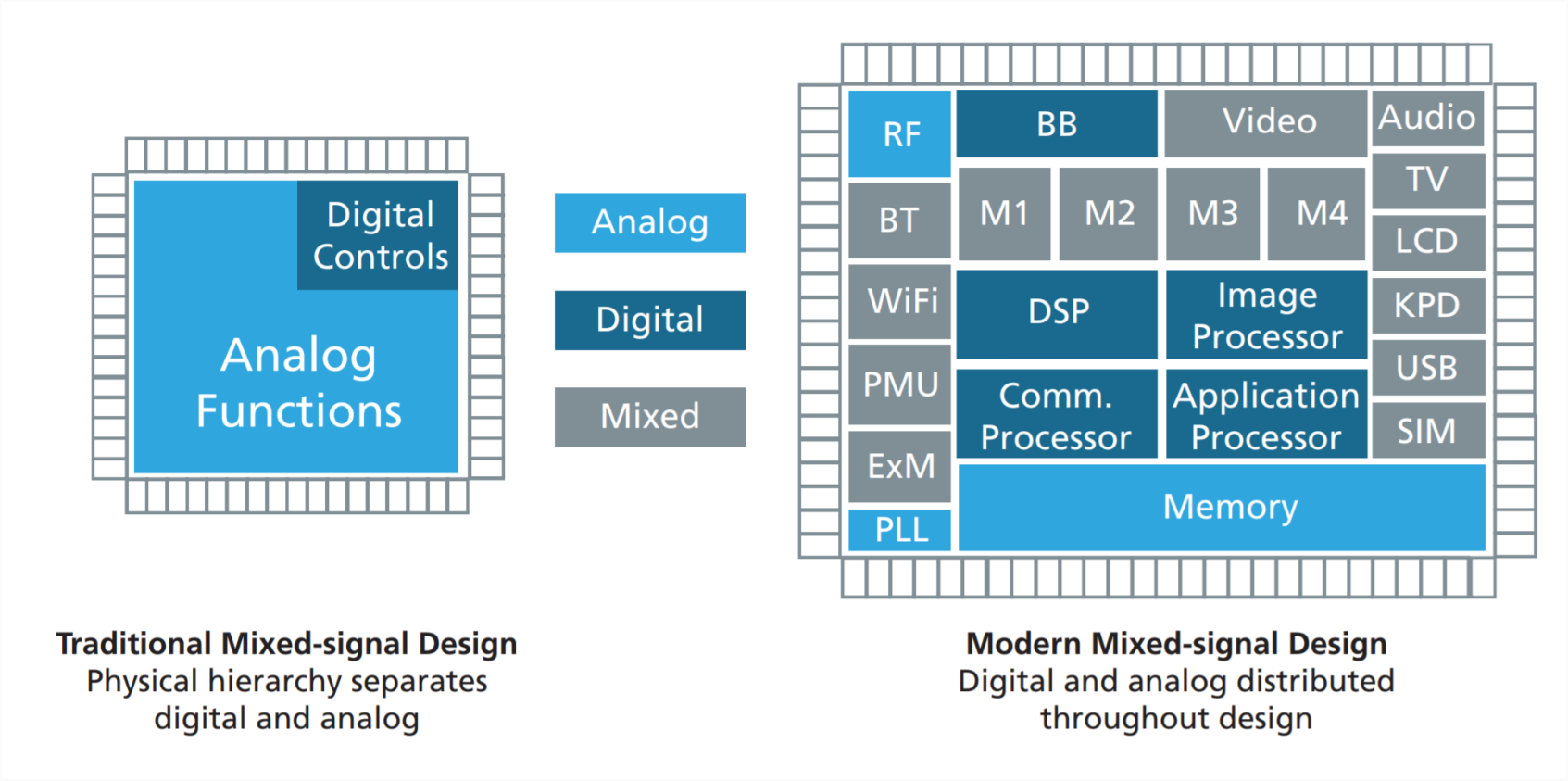

Figure 6: Increasing complexity of mixed-signal designs [**7**]

MS-SoC validation

- Mixed and more complex IPs
- Interactions and feedback loops between analog and digital IPs
- Traditional black-box approach cannot verify new designs
- Analog SPICE vs. pure digital RTL simulation
- Introducing analog behavior modeling (Verilog-AMS, System-Verilog, ...)
  - Creating functional models to allow verification / simulation
  - Real number modeling (WREAL)
  - 5 to 100 times faster
  - Taking advantage of digital simulation environment
  - SPICE is still gold standard for analog design

MS-SoC validation cont.

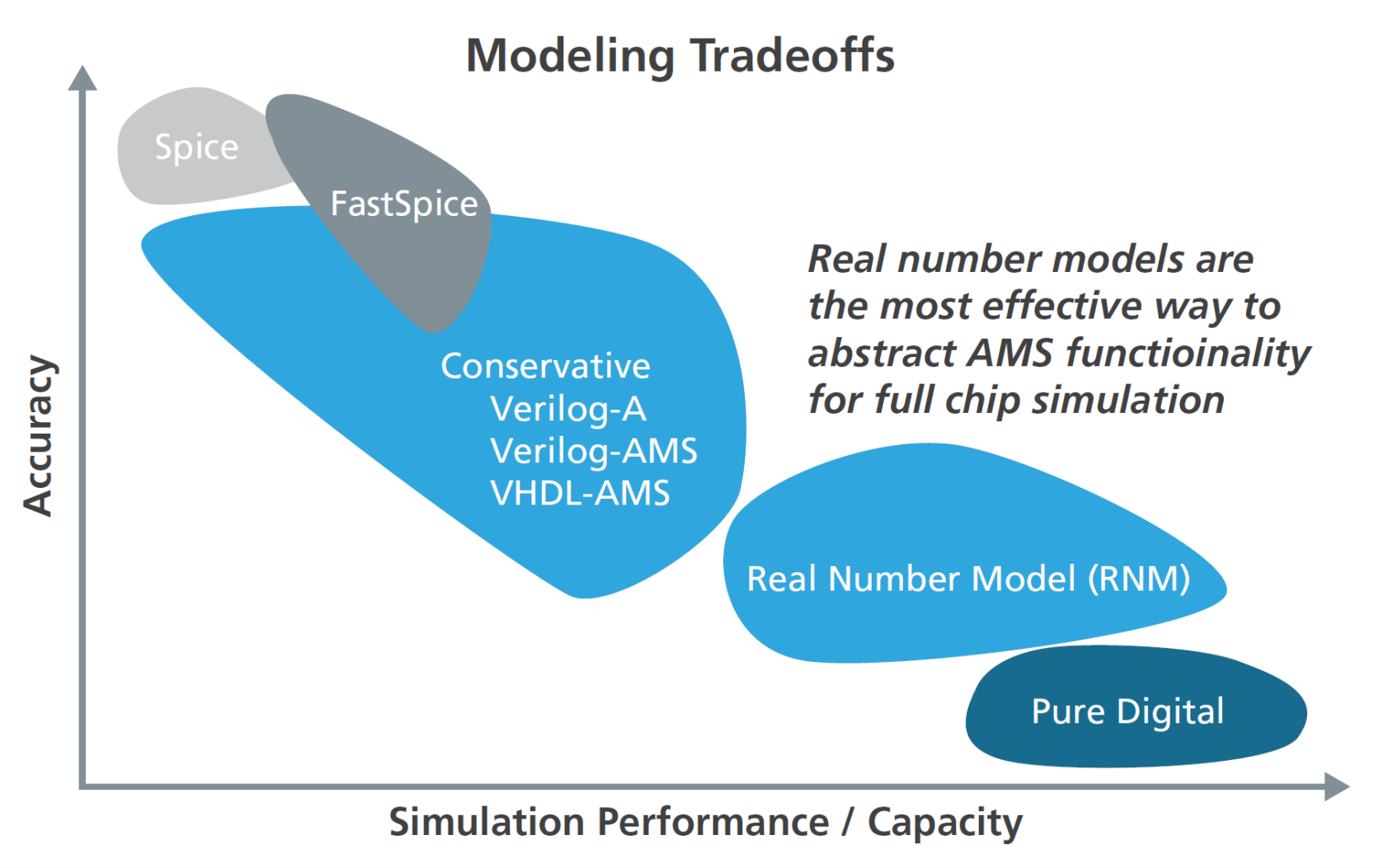

Figure 7: Modeling trade-offs [7]

VCO in Verilog AMS

```
1  module vco(vin, clk);
2    input vin; wreal vin;
3    output clk;
4    reg clk;
5    real freq,clk_delay;
6    always @(vin) begin
7      freq = center_freq + vco_gain*vin;
8      clk_delay = 1.0/(2*freq);
9    and
10   always #(clk_delay) clk = !clk;
11 endmodule
```

MS-FPGAs

MS-FPGAs

- FPGAs with analog subsystem:
  - Analog interface
  - Microcontroller or microprocessor functionality
  - Programmable logic of FPGA
  - DSP functionality
  - System integration and flexibility $\Rightarrow$ saving costs
- Concept of analog "Housekeeping"

FPGAs with analog subsystem

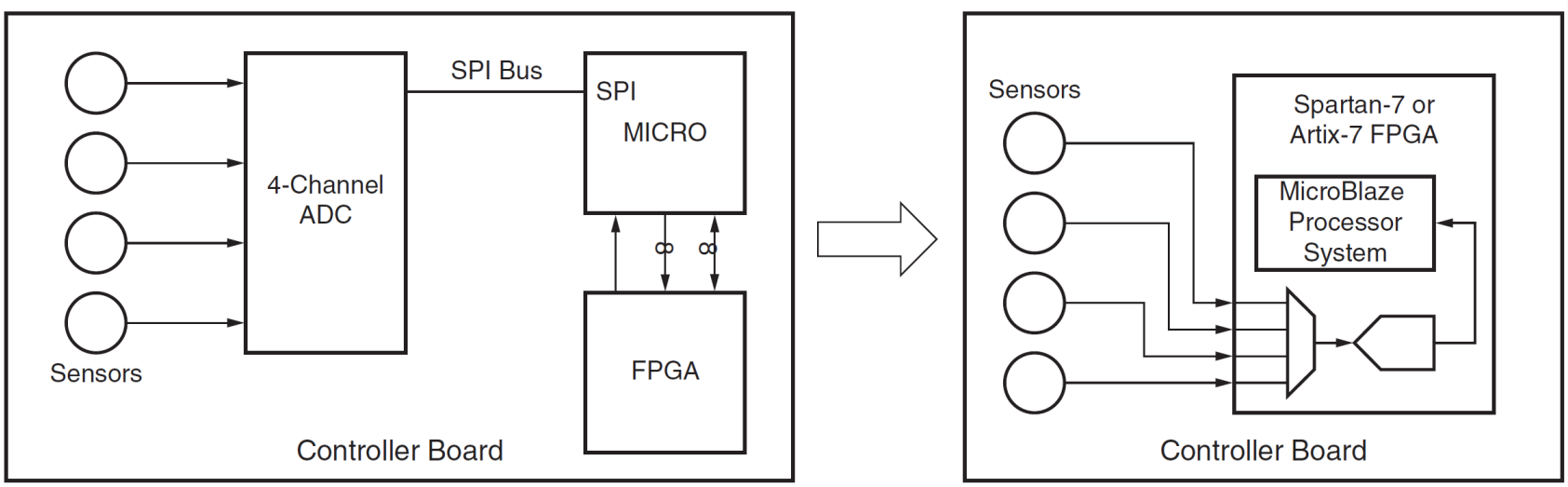

Figure 8: Concept of analog "Housekeeping" [**6**]

Zynq-7000 series

- Analog subsystem: XADC
  - 1 MSPS 12-bit ADC
  - 17-channel analog multiplexer
  - On chip temperature sensors
  - Interface to digital programmable logic
  - JTAG access to ADC measurements (ChipScope)

XADC

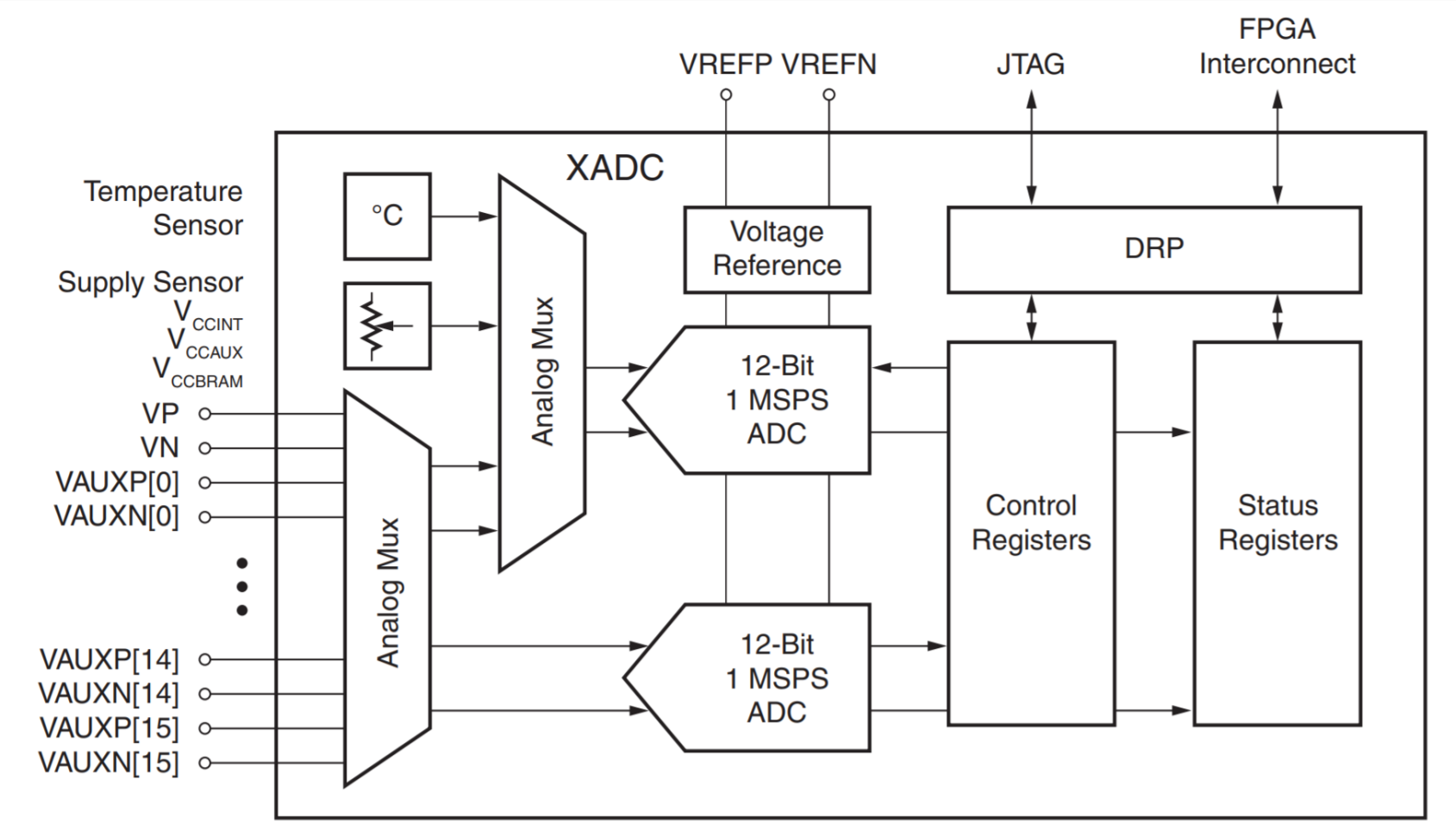

Figure 9: On chip ADC of Zynq 7000 series [**6**]

Summary

- MS-SoCs many advantages but impose huge design challenges
- Analog and digital domains are vastly different
- Several trade-offs in design flow to combine analog and digital
- MS-SoCs make analog behavior modeling necessary
- FPGAs represent "programmable" MS-SoCs
- Sometimes better solution than fully custom SoC

References i

[1] J. M. Rabaey, F. De Bernardinis, A. M. Niknejad, B. Nikolic and A. Sangiovanni-Vincentelli, *Embedding Mixed-Signal Design in Systems-on-Chip*, in Proceedings of the IEEE, vol. 94, no. 6, pp. 1070-1088, June 2006, doi: 10.1109/JPROC.2006.873609.

[2] R. Wittmann, W. Schardein, D. Bierbaum and M. Darianian, *OC-driven design methodology for full custom high performance mixed-signal designs*, Proceedings of 13th Annual IEEE International ASIC/SOC Conference (Cat. No.00TH8541), 2000, pp. 148-152, doi: 10.1109/ASIC.2000.880692.

References ii

[3] T. B. Tarim, *Mixed signal and SoC design flow requirements*, 2005 IEEE International Symposium on Circuits and Systems, 2005, pp. 5974-5977 Vol. 6, doi: 10.1109/ISCAS.2005.1466000.

[4] B. Nyambayar, K. Shiho, *A collaborative design approach to interdisciplinary mixed-signal SoCs for automotive applications*, Midwest Symposium on Circuits and Systems. 1-4. 10.1109/MWSCAS.2011.6026493.

[5] R. Landry, *Mixed Signal SoC Applications*, `https://www.design-reuse.com/articles/7333/mixed-signal-soc-applications.html`, Online; accessed 27 November 2021.

References iii

[6] A. Collins, *Xilinx Analog Mixed Signal Solutions*, https://www.xilinx.com/support/documentation/white_papers/wp392-analog-mixed-signal.pdf, Online; accessed 27 November 2021.

[7] K. Karnane, S. Balasubramanian, *Solutions for Mixed-Signal SoC Verification*, https://www.cadence.com/content/dam/cadence-www/global/en_US/documents/solutions/mixed-signal-soc-verification-wp.pdf, Online; accessed 27 November 2021.