Alternative SoC Bus Interconnections

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Why do we need buses

- Handle interconnections between units on a chip
- Reduce development cost and time
- Increase efficency
- Reduce chip size

Challenges

- Performance
- Power
- Fullfill spezifc needs
- Spezifications varying a lot

Bus Topologies

- Shared bus
- Hierarchical bus
- Ring bus
- Star bus

Signals development to Packets

- Signal based
  - Traditional Bus
  - Lots of overhead
  - Unsufficent for all needs
    - Disagreement over required features
    - Different applications require different trade-offs
- Packet based
  - Network approach
  - Interfaces, Sockets, Handshakes
  - Flow control

Soc Bus Solutions

- AMBA - ARM
- CORECONNECT - IBM
- WISHBONE - Silicore Corporation
- AVALON - Altera
- SiliconBackplane - Sonics (OCP)
- etc...

AMBA Timeline

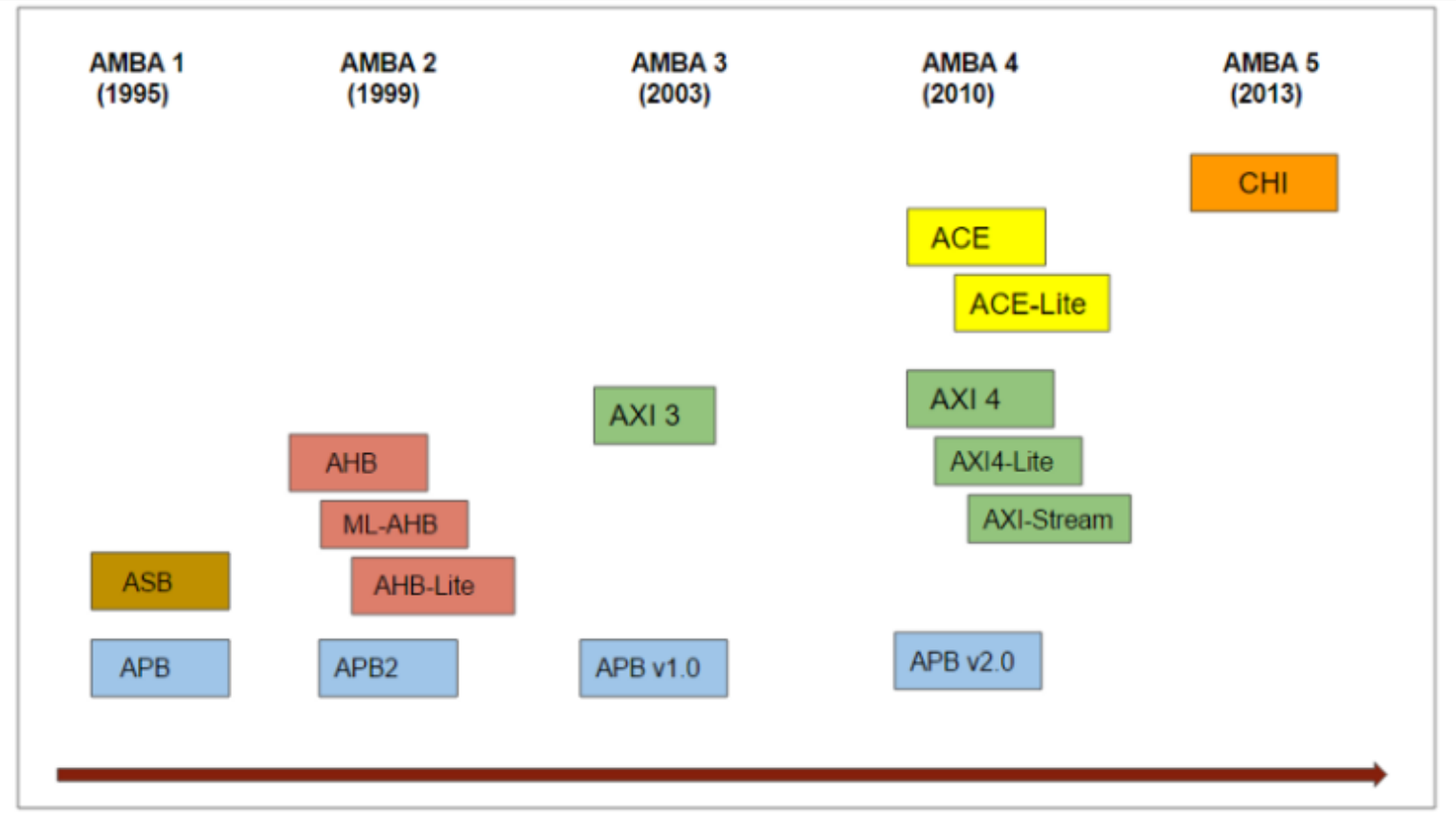


Figure 1: AMBA Protocols Timeline

Combination of multiple Protocols

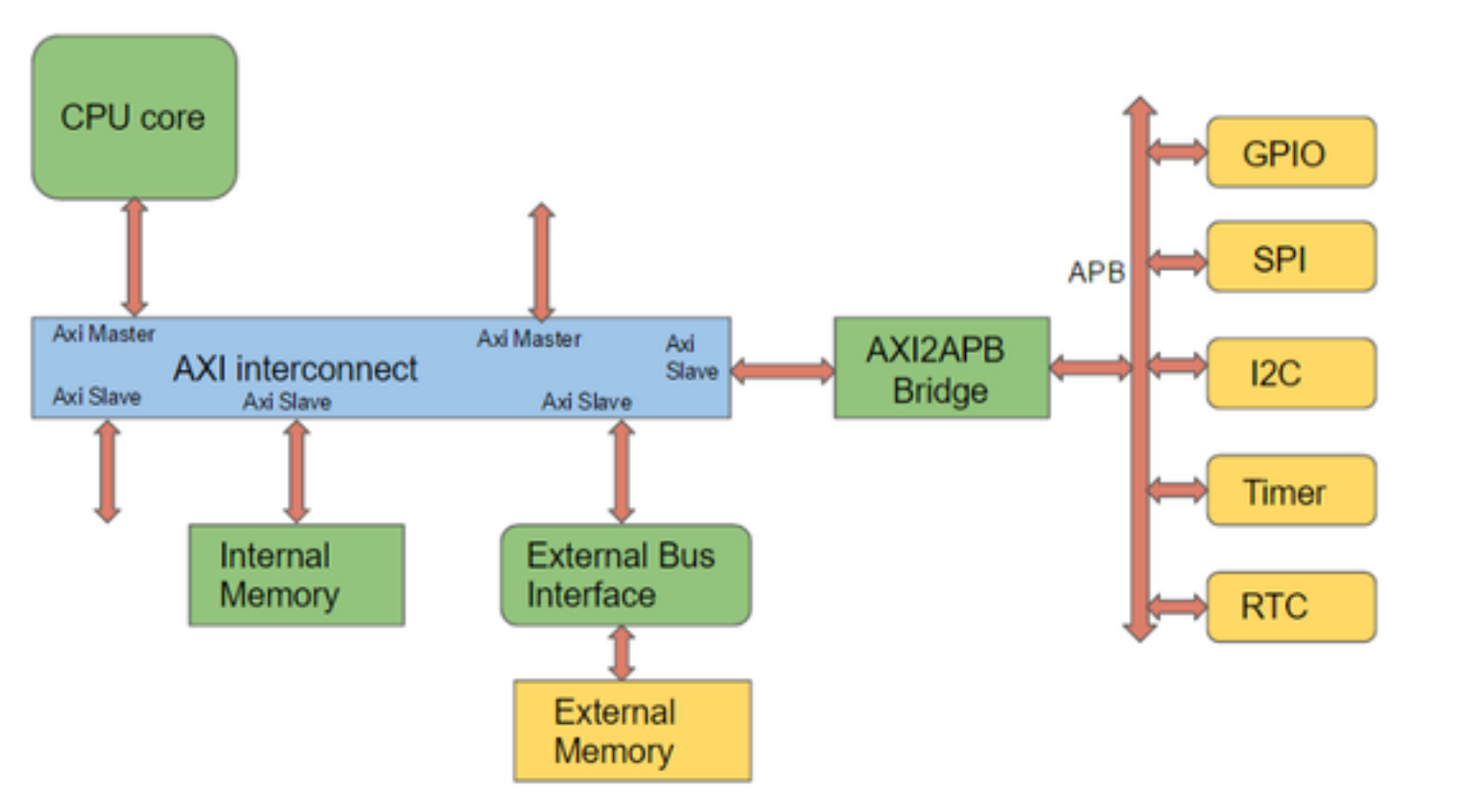


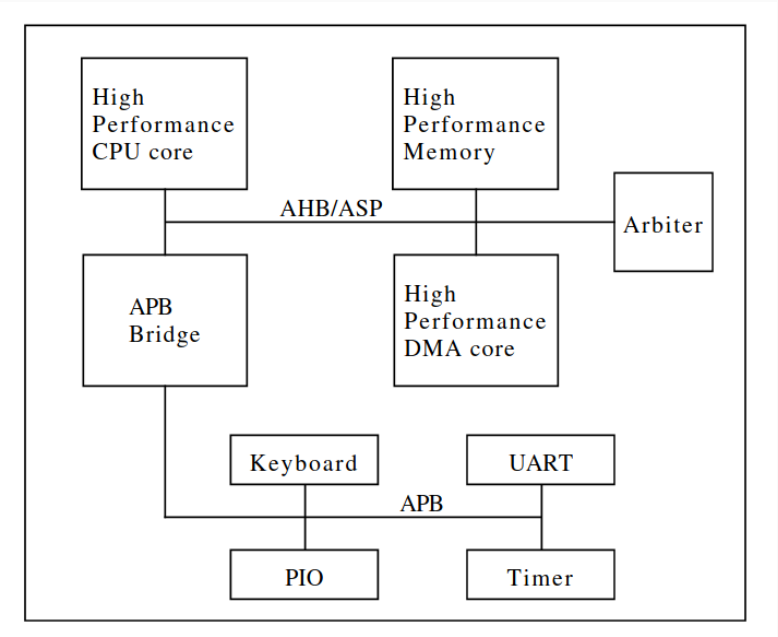
Figure 2: SoC Bus System with AMBA Protocols

AMBA 2

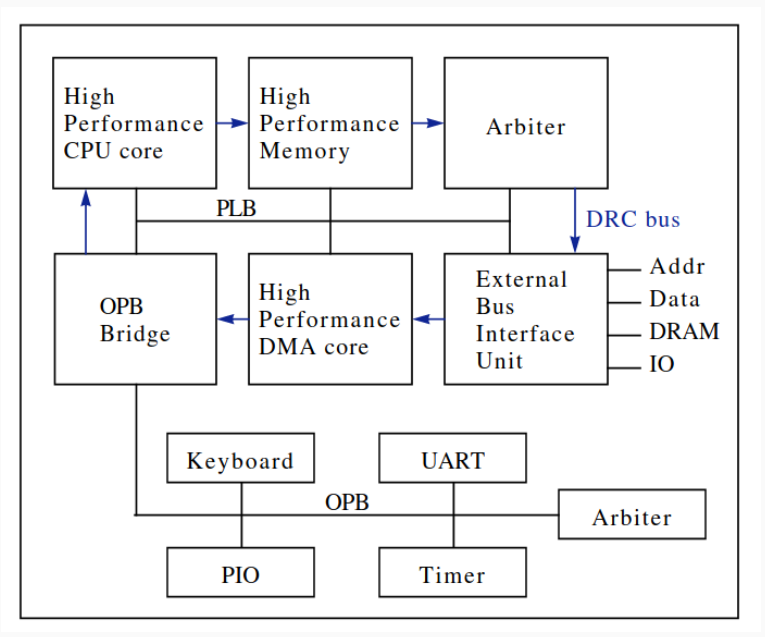
- Advanced High-Performance Bus (AHB)
  - Interconnection: multiplexed implementation
  - separate data read/write bus required
  - Burst and split transfers are supported.
- Advanced System Bus (ASB)
  - Single, tri-state data bus, unit selection signal
  - Latch-based instead of register-based design
  - Uses both clock edges
- Advanced Peripheral Bus (APB)
  - Power consumption: zero, when not in use
  - Interconnection: not defined, very simple

Amba 2 vs. CoreConnect

- Very similar and compatible
- CoreConnect has additional device control register (DCR) bus



AMBA 2 Bus System

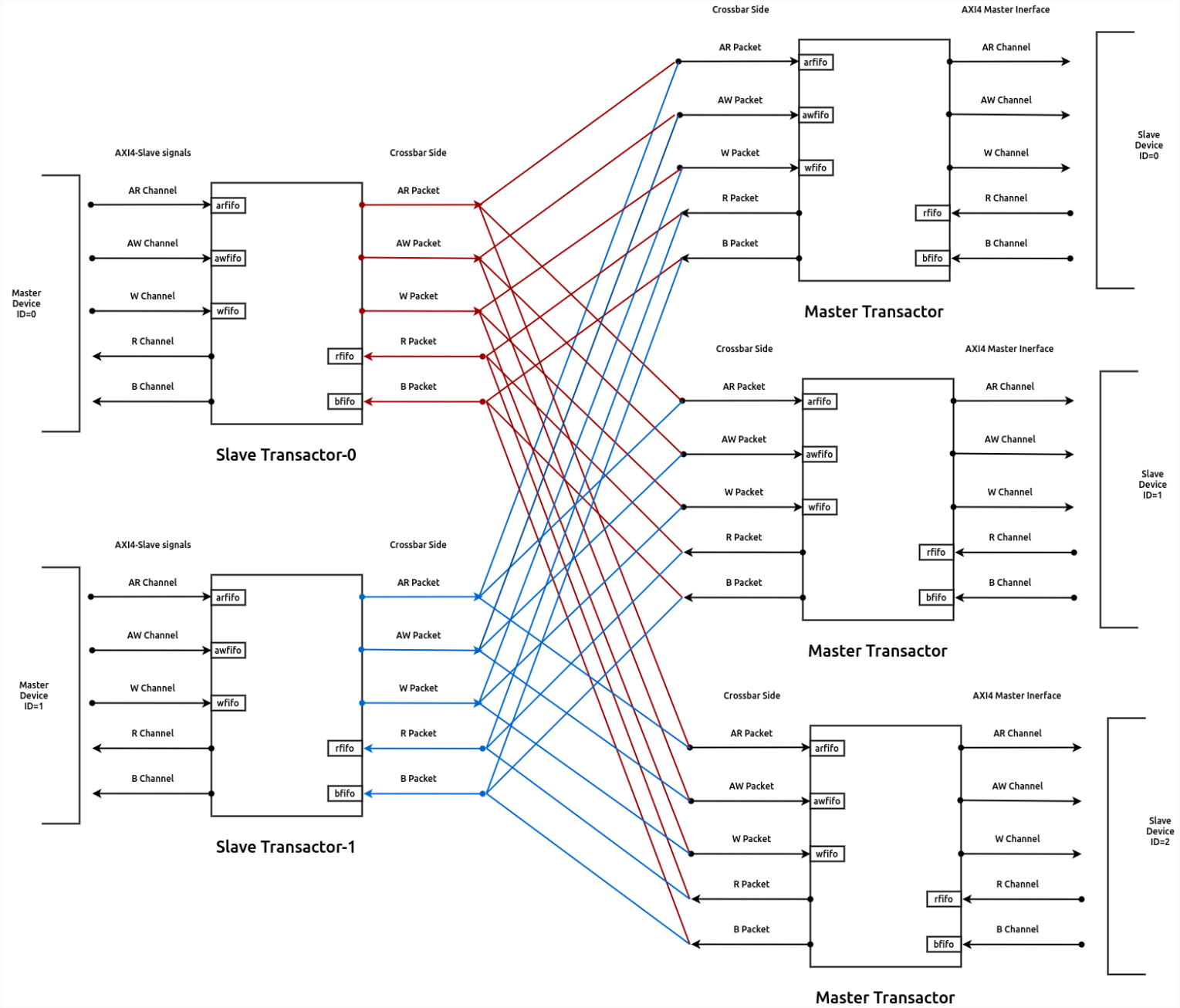


CoreConnect Bus System

AMBA 4 - AXI

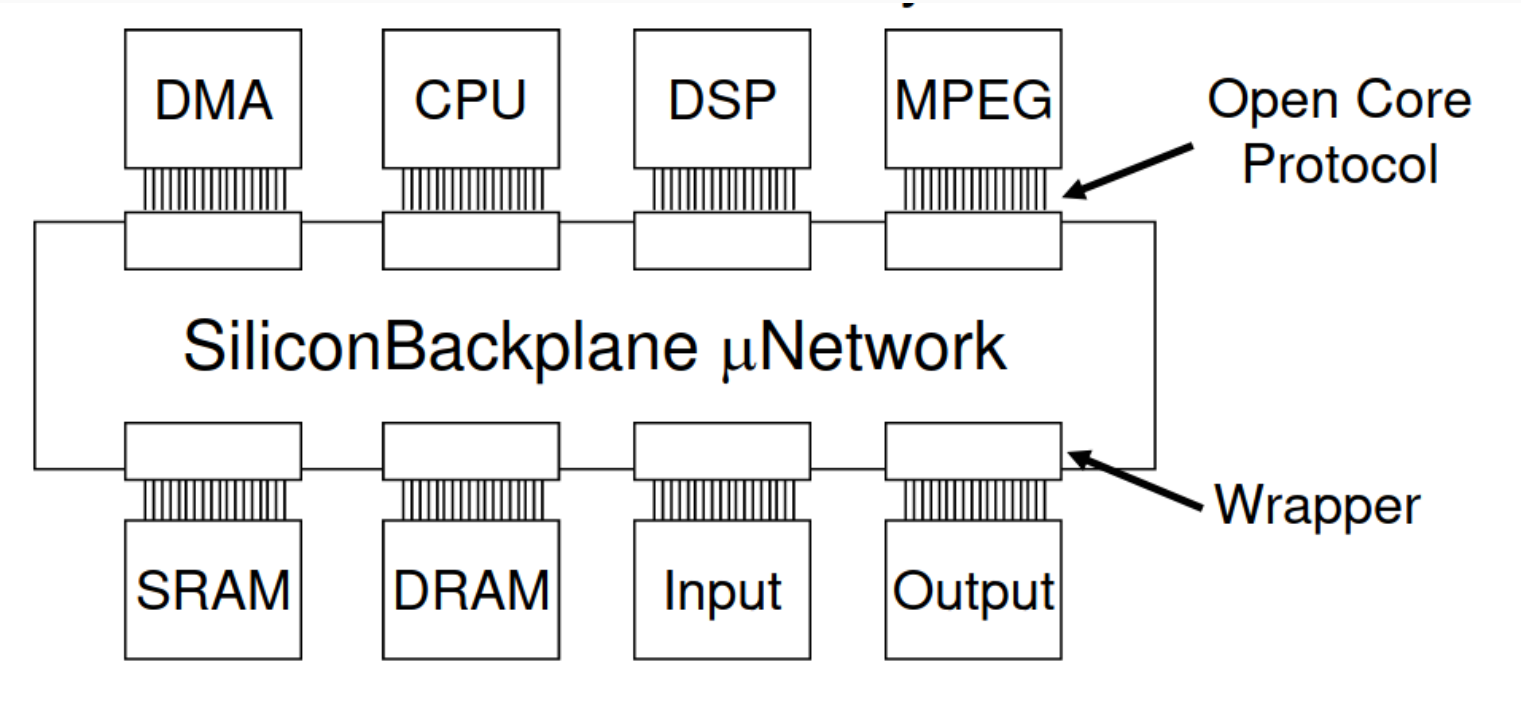
- Based on point-to-point connection concept
- separate address/control and read and write data channel
- out-of-order transaction completion

AMBA 4 - AXI


Crossbar Side
AXI4 Master Inerface
AR Packet
AW Packet
W Packet
R Packet
B Packet
arfifo
awfifo
wfifo
rfifo
bfifo
AR Channel
AW Channel
W Channel
R Channel
B Channel
Slave Device ID=0
Master Transactor
AXI4-Slave signals
Crossbar Side
Master Device ID=0
Slave Transactor-0
Crossbar Side
AXI4 Master Inerface
Slave Device ID=1
Master Transactor
AXI4-Slave signals
Crossbar Side
Master Device ID=1
Slave Transactor-1
Crossbar Side
AXI4 Master Inerface
Slave Device ID=2
Master Transactor

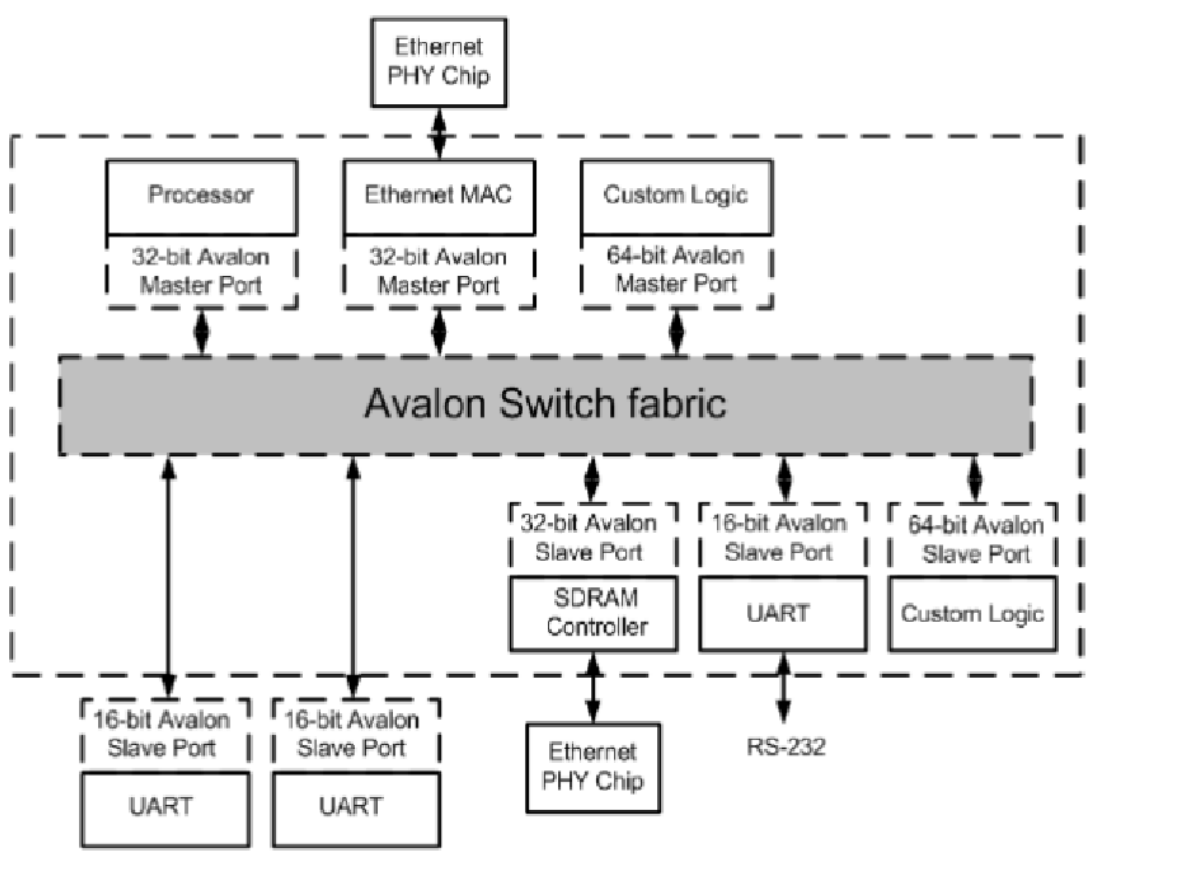
SiliconBackplane microNetwork

- Individual bus width, frequency, or electrical loading changes of IPs
- Open Core Protocol (OCP) wrapper
- optional extensions to the basic OCP for reset, interrupts, errors, control/status information



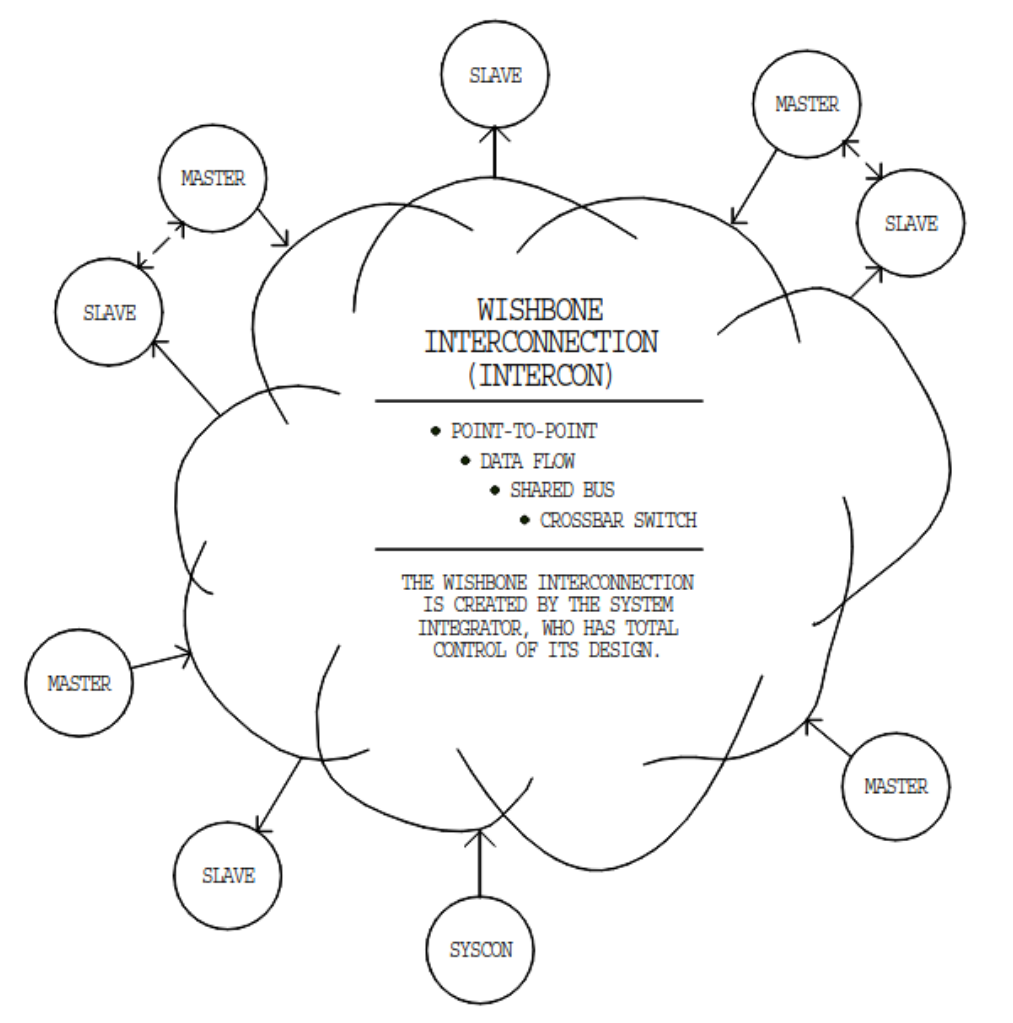
Altera Avalon Bus

- Altera devices only using SOPC Builder tool
- Burst, wait-state generation, interrupt-priority assignment
- Tristate (devices with a shared read/write channel)

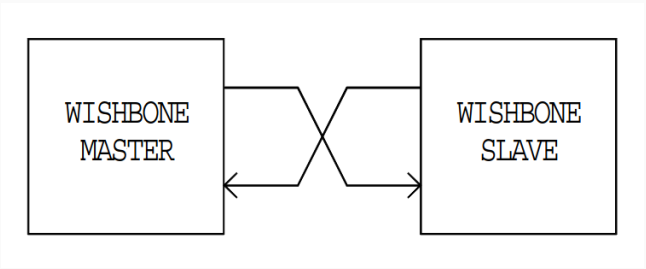


Wishbone

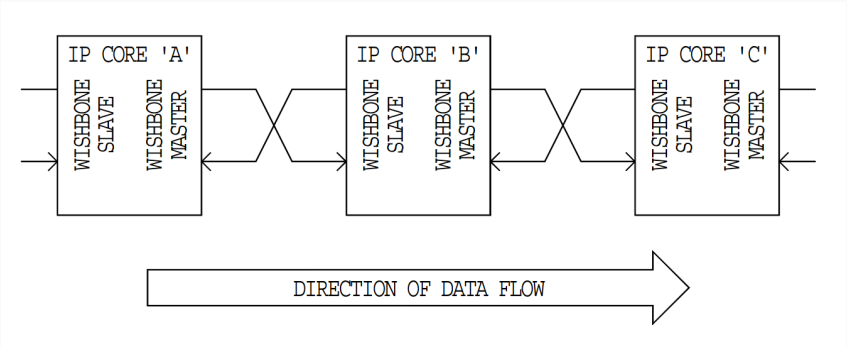
- Very simple and modifiable
- off-the-shelf INTERCON
- possible off-chip interconnection



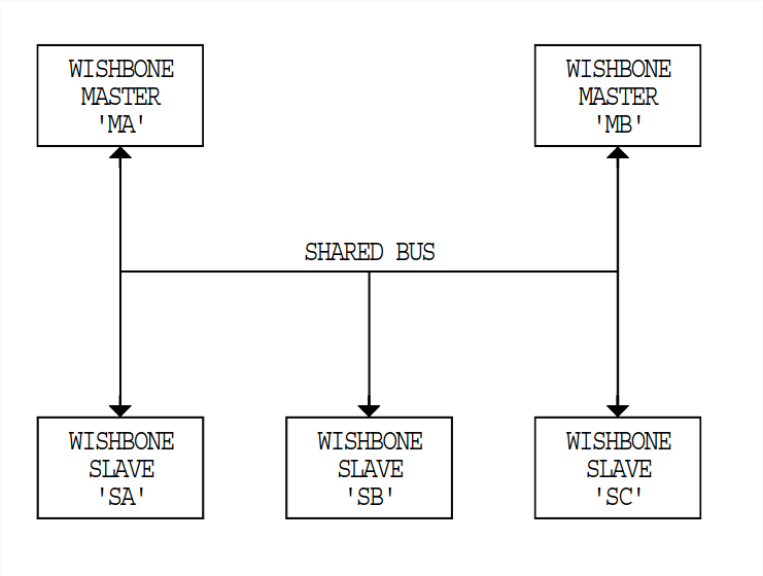
Wishbone Toplogies



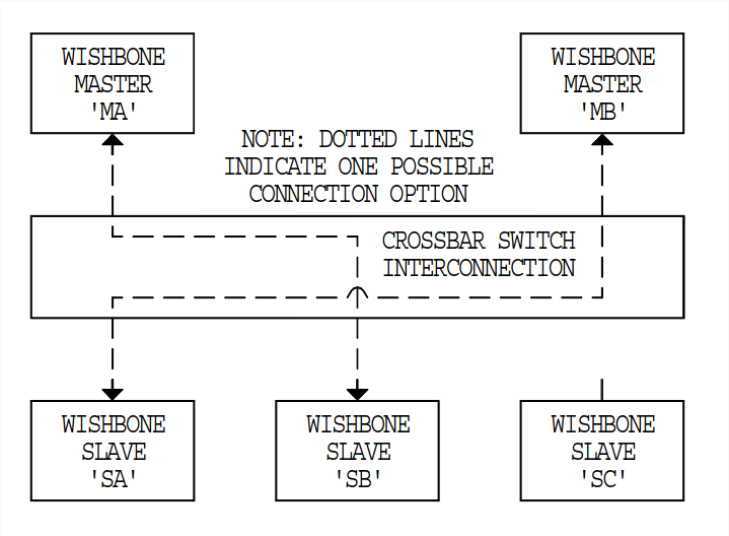
P2P interconnection



Data-flow interconnection



Shared bus interconnection



Crossbar interconnection

AMBA 5 - CHI (Coherent Hub Interface)

- support multiple CPU cores
- complete re-design of AXI/ACE
- layered packet based communication protocol
  - link layer and physical layer
- flow control, cached routing
- interconnecting designs ranging from an efficient, small cross-bar to high performance, large scale mesh network

References i

- Shaahin Hessabi. *SoC Design Lecture 11: SoC Bus Architectures*. `http://ce.sharif.edu/courses/88-89/1/ce757-1/resources/root/Slides/lec11.pdf`. Online; accessed 28 October 2021.
- Richard Herveille, OpenCores Organization. *WISHBONE System-on-Chip (SoC) Interconnection Architecture for Portable IP Cores*. `https://cdn.opencores.org/downloads/wbspec_b3.pdf`. Online; accessed 28 October 2021.

References ii

- Verification Excellence. *Understanding AMBA Bus Architecture and Protocols*. `http://verificationexcellence.in/amba-bus-architecture/`. Online; accessed 28 October 2021.
- InCore Semiconductors. *AXI4 Cross-bar Interconnect*. `https://fabrics.readthedocs.io/en/latest/axi4_crossbar.html`. Online; accessed 28 October 2021.