FPGAs in Space

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Example Frame Title

- History
- Challenges and Risks
- Political Challenges
- Specialized Hardware
  - FPGAs developed for Space
  - Remote FPGA Configuration
  - Testing Hardware with FLIPPER
- Lessions Learned

History

First Usage

- At first only ASIC were used.
- Very Large Scale integration "VLSI"
  - 1985 First ASIC from NASA for ground telemtry processing at the Goddard Space Flight Center
  - magnitude improvement in performance, cost and size over previous telemetry processing implementations
- VLSI-based system lead to a wide spread usage of ASICs
  - Small Explorer missions, Deep Space Network, Hubble Space Telescope

First real FPGA in Space

- First FPGA was used in the SAMPEX data processing unit (DPU)
- SAMPEX was launched on July 3, 1992 from Vandenberg Air Force Base into a 550 x 675 km orbit.
- Harris 80C85RH microprocessor
- 12 Actel FPGAs
  - 2000 logic gates
  - 2.2 cm^2
  - each 102mW power usage

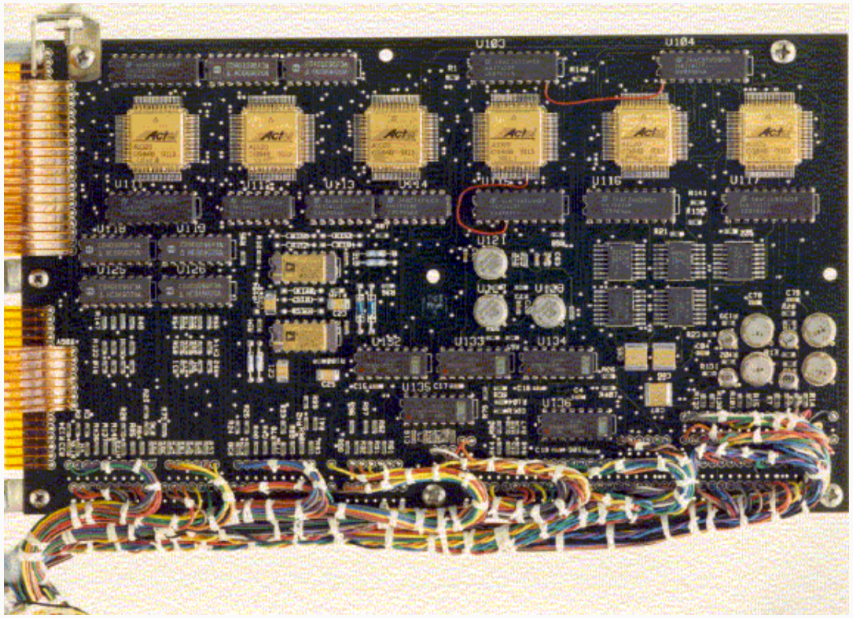

Figure 1: SAMPEX data processing unit

FPGA in Space

- FPGAs where used more with time
- Advantages
  - Increasing integrated circuit design costs
  - FPGA offers time-to-market advantage
- Disadvantages
  - High volume applications
  - Higher power consumption compared to ASIC

FPGA in Space

- 2008 Immarsat 4 communication satellite
- 2018 BepiColombo Mercury Planetary Orbiter

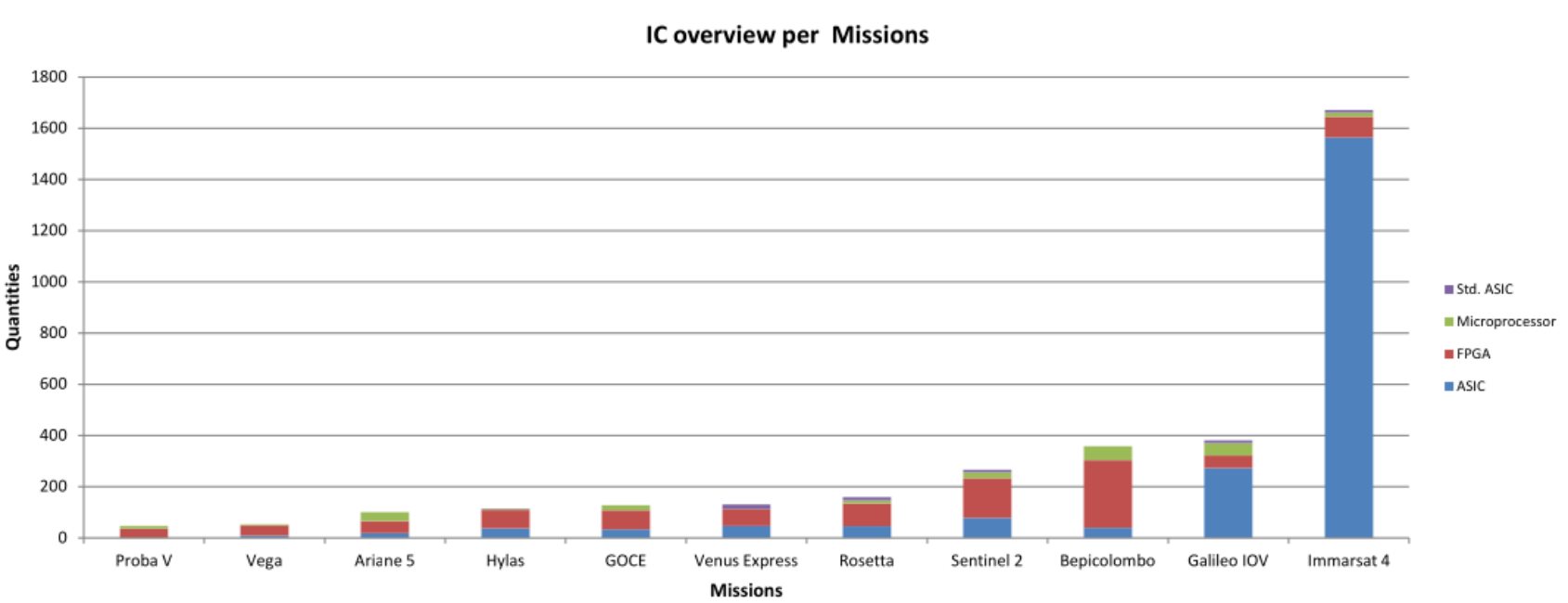

Figure 2: Image from **tren2012Rog**

FPGA in Space

- 2013 Proba V Earth observation for vegetation observation

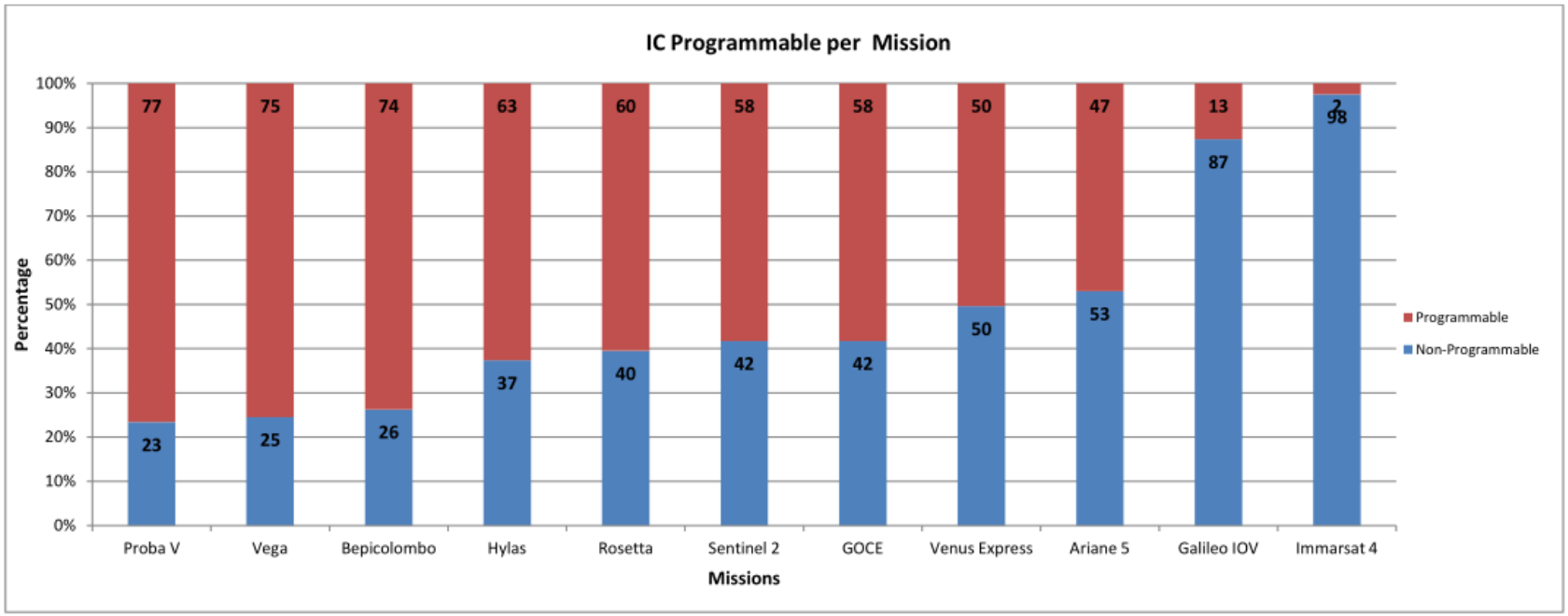

Figure 3: Image from **tren2012Rog**

FPGA in Space

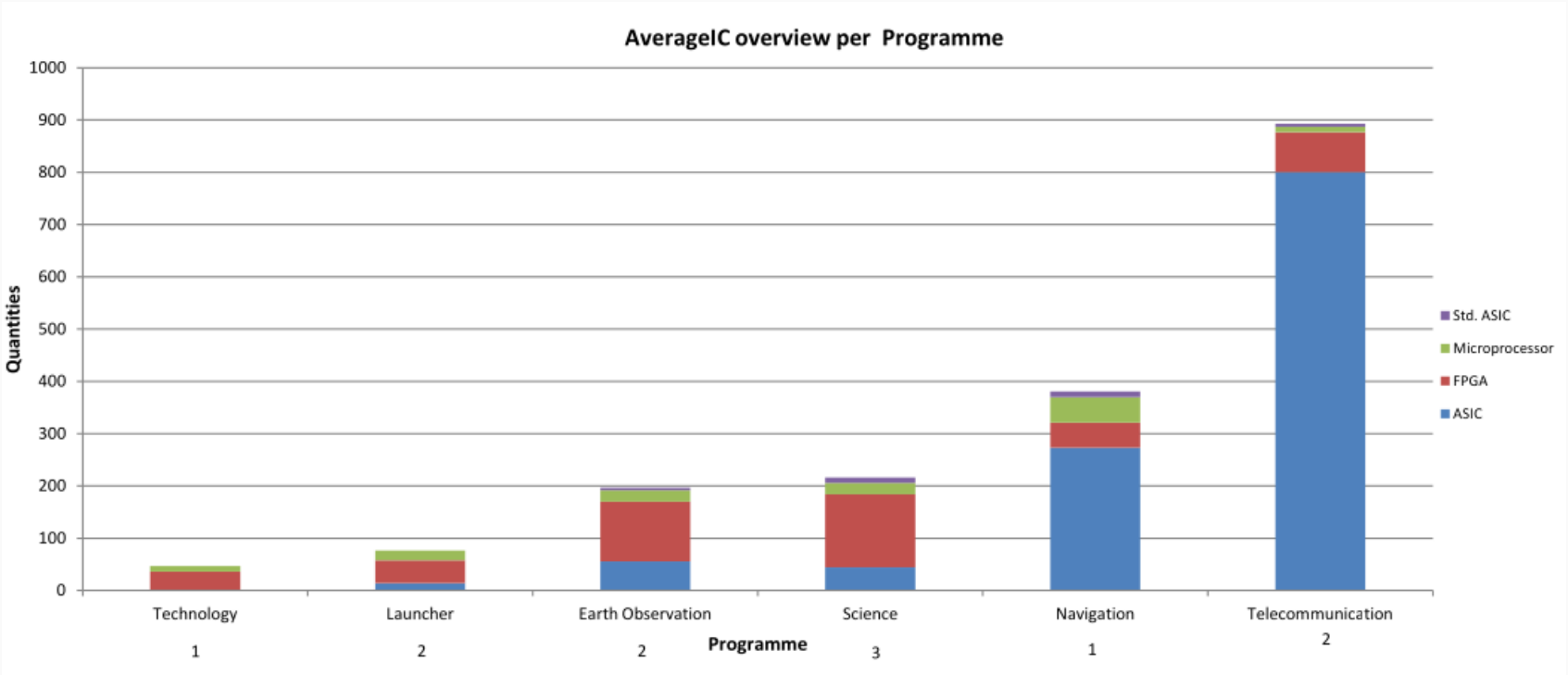

Figure 4: Image from **tren2012Rog**

FPGA in Space

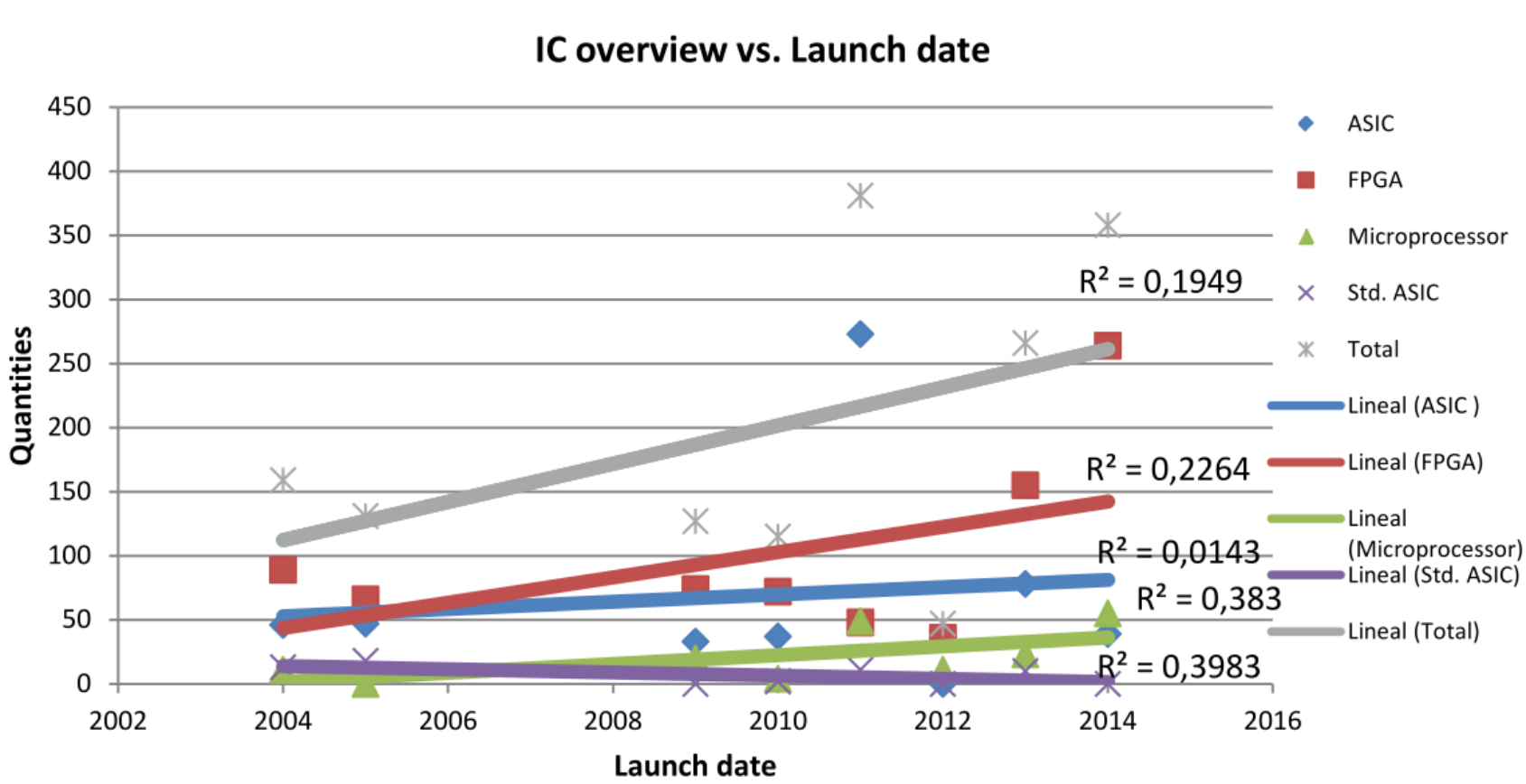

Figure 5: Image from **tren2012Rog**

Relative quantities

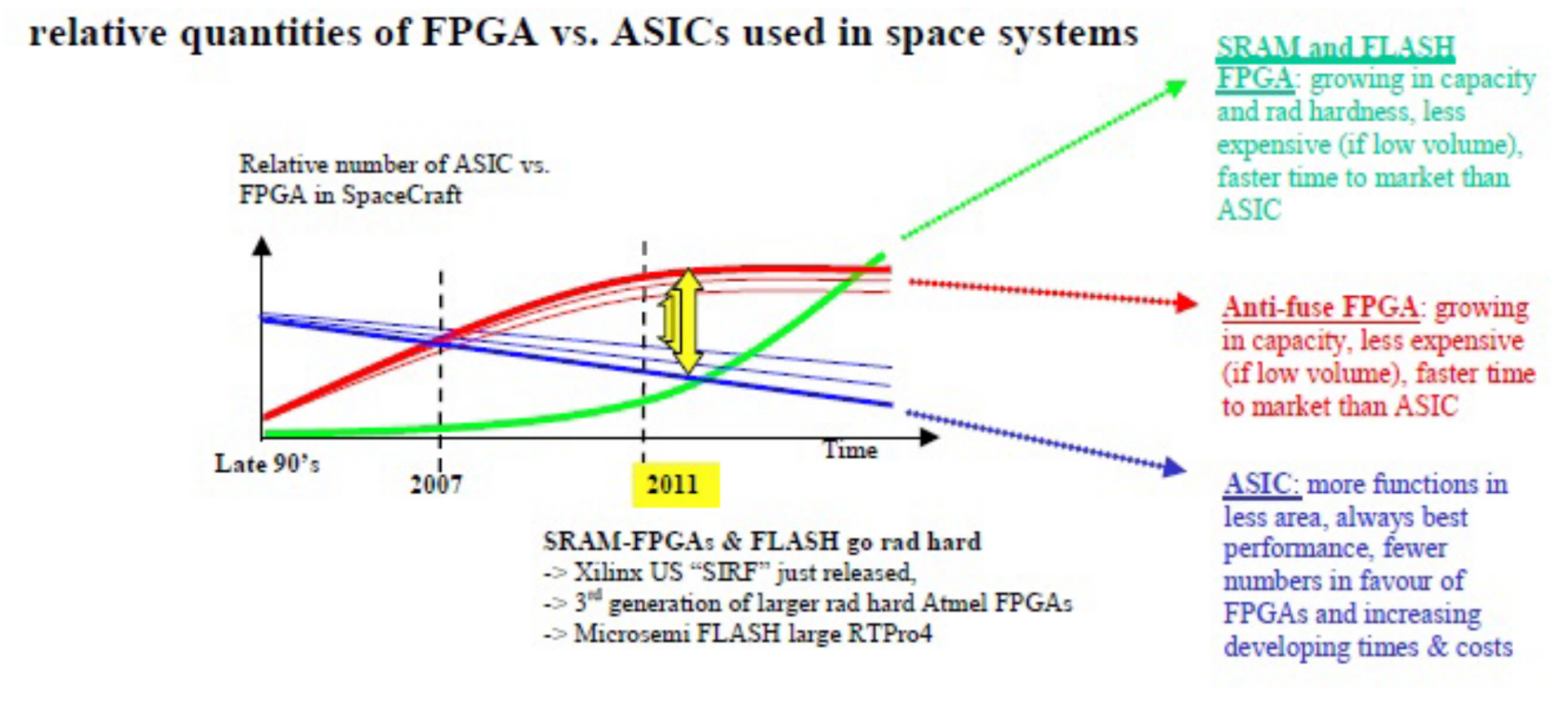

Figure 6: Usage of FPGA and ASIC over time

Challenges and Risks

Single Event Upsets (SEU)

- Single Event Upsets (SEU)
  - Caused by radiation
- Have affects on registers and memory
- therefore they affect the functionality of the combinatorial logic

Mitigation

- straight forward mitigation is "Triple Modular Redundancy" for all registers
- does not protect on-chip memory or against multiple upsets

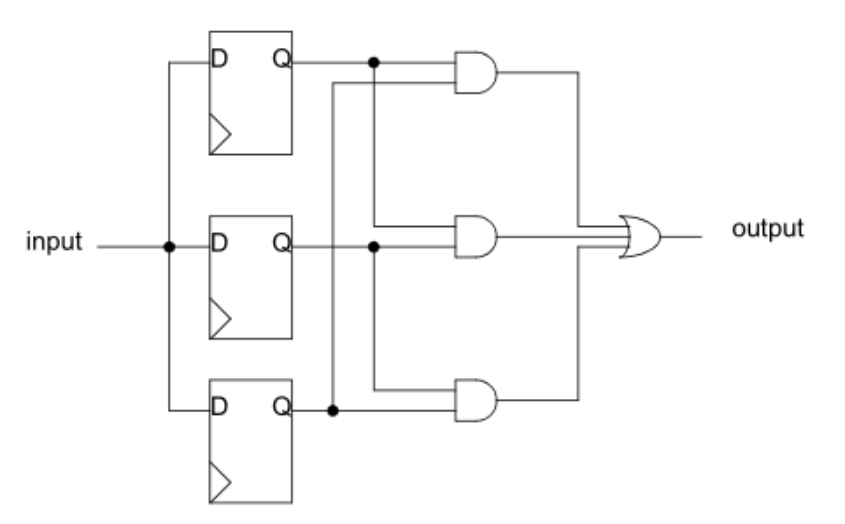

Figure 7: Voting of 3 registers

- also works at higher levels: Use 3 FPGAs, reprogram the faulty one

Mitigation

- Use idle cycles in the design for concurrent error detection
  - Prototyped using a Xilinx Virtex
- Automatic protection mechanisms for registers and memory in code
  - Mechanisms based on Hamming coding and two dimensional parity arrays
  - Approach has been demostrated using Altera and Xilinx devices **suit2002Sandi**

Mitigation

- Using Silicon on insulator (SOI) transistors
  - Used for radiation-sensitive applications
  - Better protection against SEU/radiation
- Lot of other Hardware based optimizations
  - Different memory technologies, directional routing...

Political Challenges

Political Challenges

- All major space FPGA suppliers are US companies
- Space parts must be checked by US International Traffic in Arms Regulation (ITAR)
- If technologies are protected Information is restricted to US citizens
- ITAR is an intend to stop American technology falling into enemy hands
- ESA complained that these restrictions complicate project management

Specialized Hardware - FPGAs developed for Space

Xilinx FPGAs for Space

- Xilinx offers different product families
- Normal, Dfense Grade and Space Grade
- Space Grade is normally a few generations behind
- Latest Space Grade Xilinx FPGA "Kintex UltraScale" was introduced 2014 for normal usage

Xilinx FPGAs for Space

- Are used in many satellites
  - Iridium Next (US, 66 active satellites)
  - Glonass-K (Russian space-based satellite navigation system)
  - NovaSAR-S
- Used in research satellites because they are "On-Orbit Reconfigurable"

RT Kintex UltraScale

- 20nm (previous Space-Grade FPGA Virtex-5QV was 64nm)
- 38mb memory
- Lots of communication hardware
- Radiation-Effects Mitigation and Hardness
  - Layout of the configuration memory cells is optimized with SEU design rules
  - Users can enable build-in tools for more hardness like triple modular redundancy and error detection
  - periodic device reconfiguration

RT Kintex UltraScale

- Own configuration engine for periodic reconfiguration

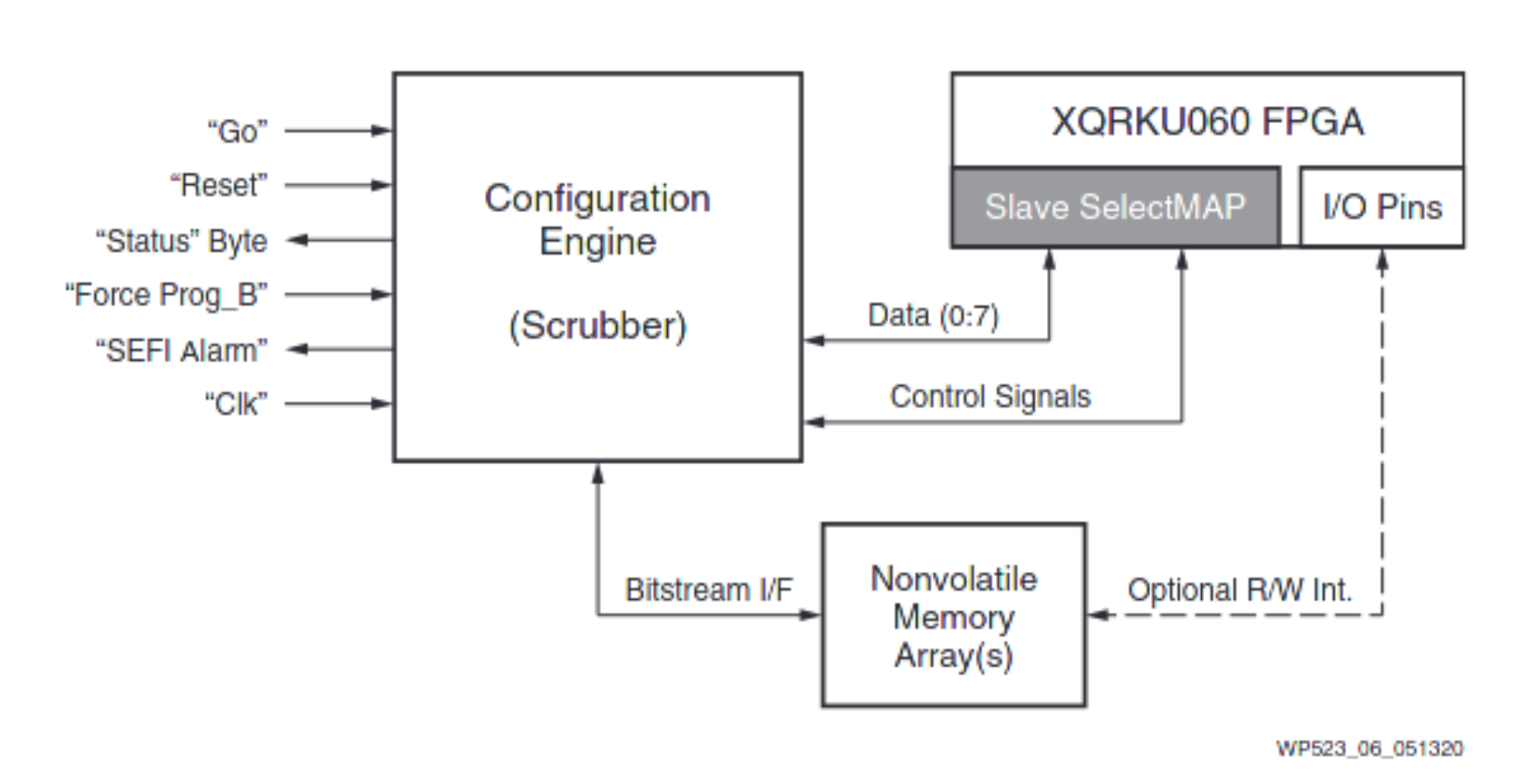

Figure 8: Image from **kin2020xil**

RT Kintex UltraScale

- Radiation Characteristics

Symbol	Description	Min	Typ	Max	Units
TID	Total Ionized Dose (GEO)	-	100	120	Krad (Si)
SEL	Single-Event-Latch-Up Immunity	-	80	-	MeV-cm2/mg
SEUCRAM	Single-Event Upset in Configuration RAM (GEO)	-	1.0e-8	-	Upset/bit/day
SEUBRAM	Single-Event Upset in Block RAM (GEO)	-	8.5e-9	-	Upset/bit/day
SEFICRAM	Single Event Functional Interrupt Orbital Upset Frequency – Configuration RAM (GEO)	-	4.5e-4	-	Upset/device/day

Figure 9: Image from **kin2020xil**

RT Kintex UltraScale

- Can utilize the TMR idea
- Implemented using software IPs (3x 32bit RSIC processors)

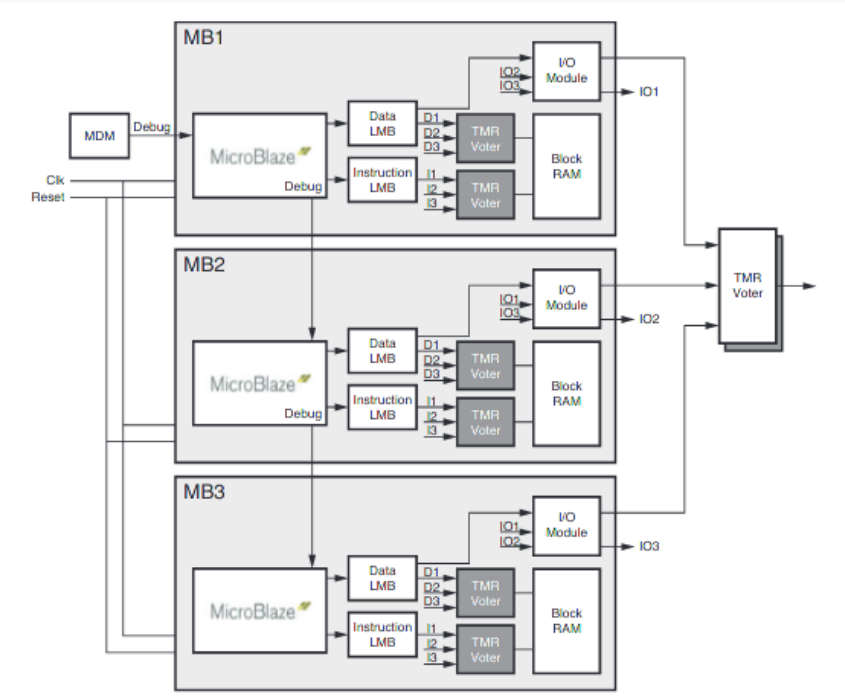

Figure 10: Image from **kin2020xil**

Specialized Hardware - Remote FPGA Configuration

CFTP

- Configurable Fault Tolerant Processor
- Project from Naval Postgraduate School
- Same FPGA two times, one for experiments
- Allows simple experiments and tests with FPGAs in Space

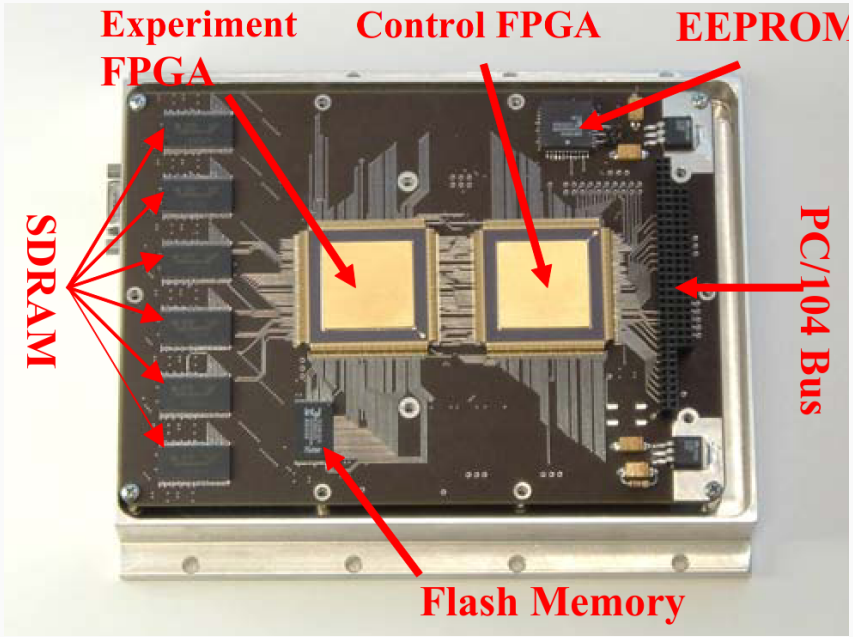

Figure 11: Image from **chal2005sur**

Specialized Hardware - Testing Hardware with FLIPPER

FLIPPER

- Project founded by ESA
- Emulates fault emulation for SRAM-based FPGA devices
- Acomplished by partial reconfiguration
- Two major releases, latest one with Virtex-5

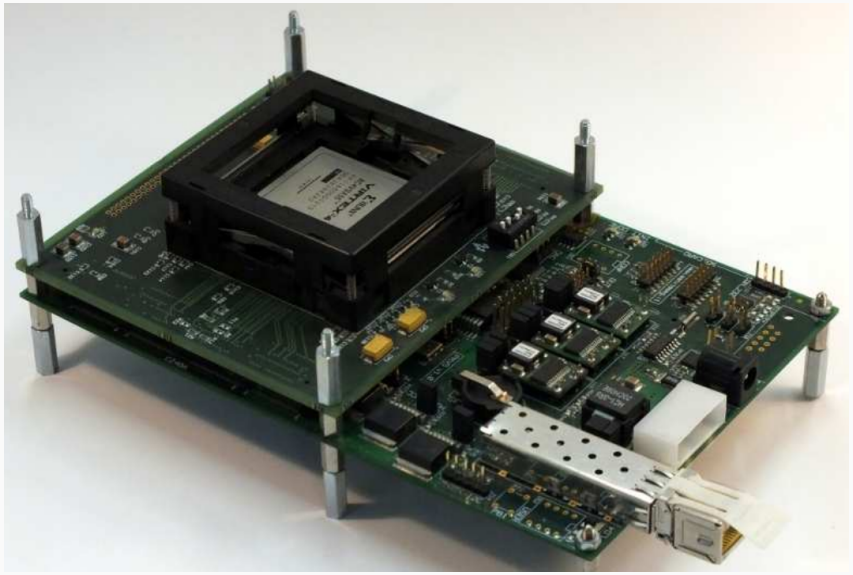

Figure 12: Flipper with Xilinx Virtex-4, Image from **isaf2017Flipper**

FLIPPER

- Quantitative characterization of design robustness
- Can be used for comparison of design hardening techniques
- Tuning of design redundancy and protection

Lessions Learned

The Single Event Upset review

- In a recent satellite project a task force was formed to investigate FPGA desings in critical systems **less2002Sandi**
- Conclusions:
  - Designers are often unaware of how the synthesis tools work
  - Little effort had been done to verify that SEU protection were actually implemented
  - It is extremely costly to perform a review a long time after the design has been completed
  - Poor awareness in spacecraft projects regarding the sheer number of FPGA designs and parts used on spacecrafts

The WIRE power-up mishap

- WIRE - Wide-field Infrared Explorer (also Explorer 75 and SMEX-5)
- NASA satellite
- The FPGA on board was a synchronous reset
- Startup time for the oscillator was not taken into consideration
- Default values during startup where not checked
- The telescope cover came off prematurely and the telescope was unusable

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