Architecture of FPGAs

Meinhard Kissich

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Agenda

- Introduction
- Overview
- Configurable Logic Blocks (CLBs)
- (CLB) Slices
- Interconnect Resources
- SelectIO Resource
- FPGA Configuration
- Other Resources

Introduction

Definition

What is the presentation about:

- Introductional overview of FPGA resources
- Purpose of resources
- Pointers where to continue reading (**Xilinx User Guides!**)

What is the presentation **not** about:

- Deep insight
- Hands-on

Overview

Big Picture

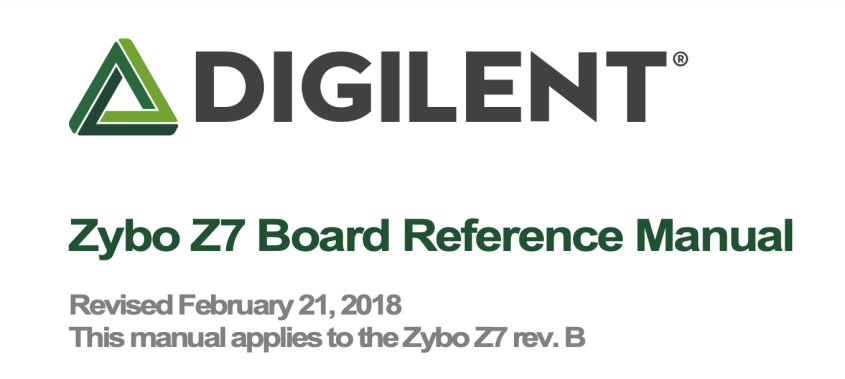


Figure 1: Zybo Z7 reference [1, p. 1].

Big Picture

ZYNQ Processor

- 667 MHz dual-core Cortex-A9 processor
- DDR3L memory controller with 8 DMA channels and 4 High Performance AXI3 Slave ports
- High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO
- Low-bandwidth peripheral controllers: SPI, UART, CAN, I2C
- Programmable from JTAG, Quad-SPI flash, and microSD card
- Programmable logic equivalent to Artix-7 FPGA

Figure 2: Zybo Z7 specs [1, p. 3].

Xilinx 7-Series

- Spartan-7: low cost, low power
- Artix-7: low power, high throughput
- Kintex-7: best price-performance
- Virtex-7: highest system performance

Same CLBs in all (7-series) FPGA families [3]

Big Picture

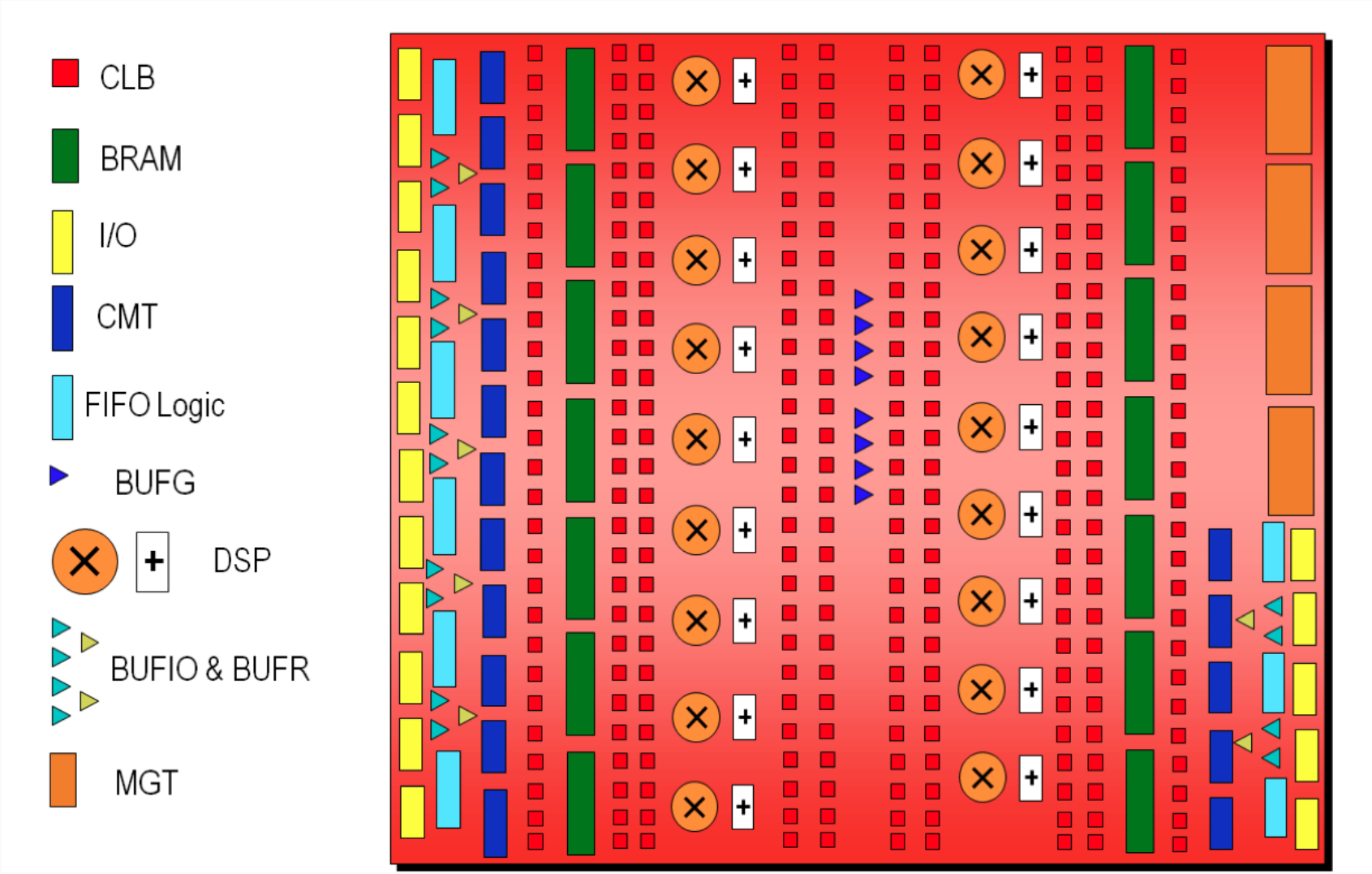


Figure 3: Overview 7 series (ASMBL) architecture [2, p. 9].

Configurable Logic Block (CLB)

Configurable Logic Block

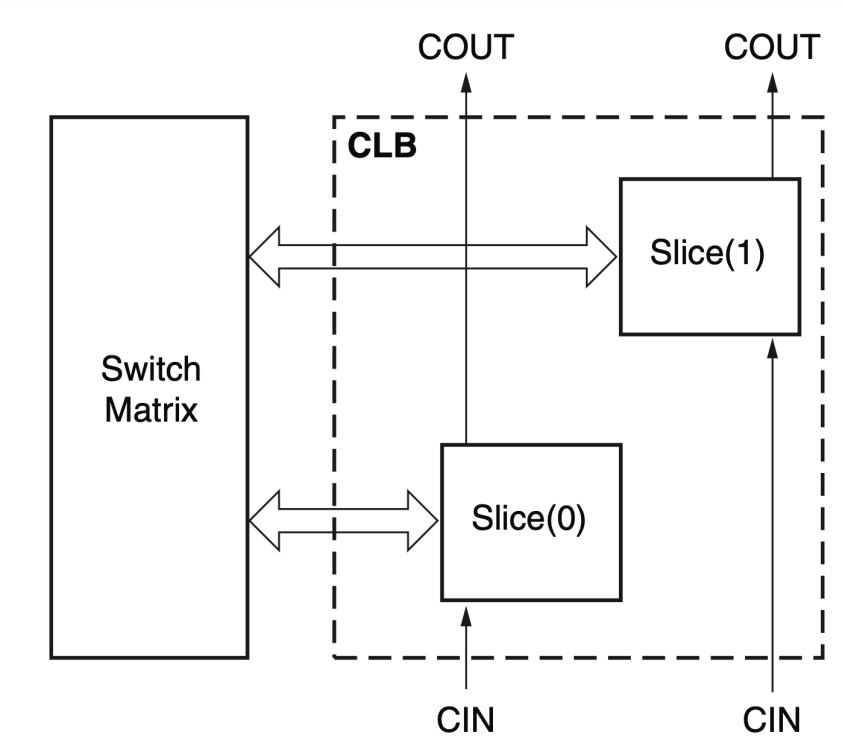


Figure 4: CLB and slices [3, p. 9].

- CLBs arranged in columns (ASMBL)
- Connected to switch matrix
- Contains a pair of slices
- No direct connection, each slice organized as a column
- $2 \times$ SLICEL or SLICEL + SLICEM

CLB Slices

- 4 × 6-input LUTs
  (or 8 × 5-input)
  (= logic-function generators)
- 8 × flip-flops (storage unit)
- Multiplexers
- Arithmetic carry logic

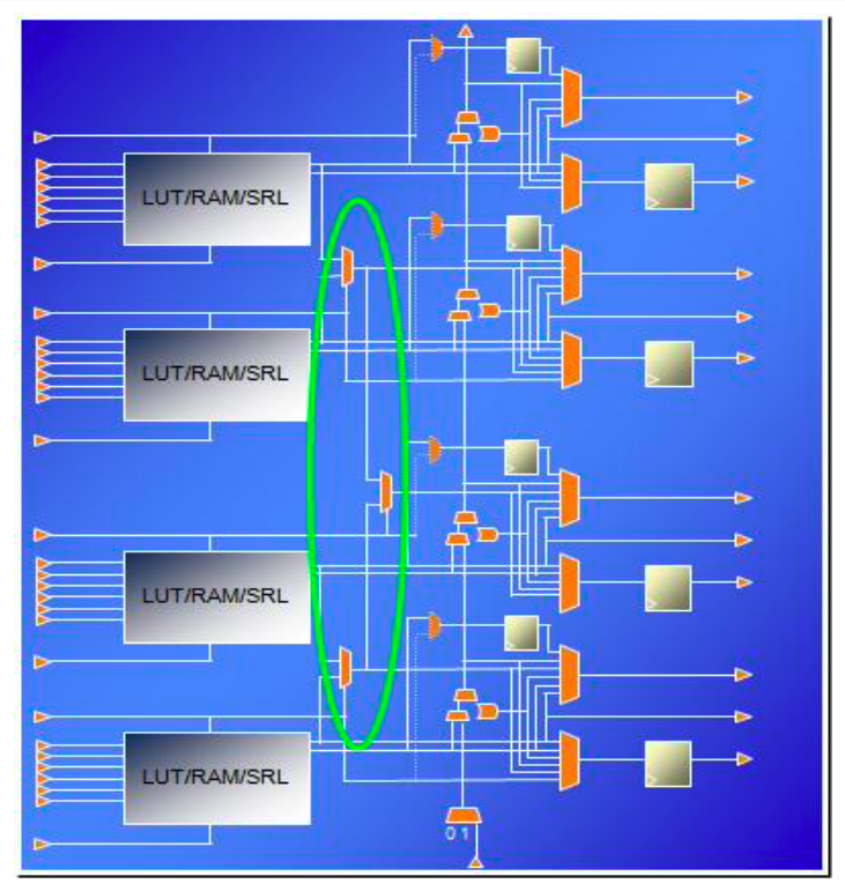
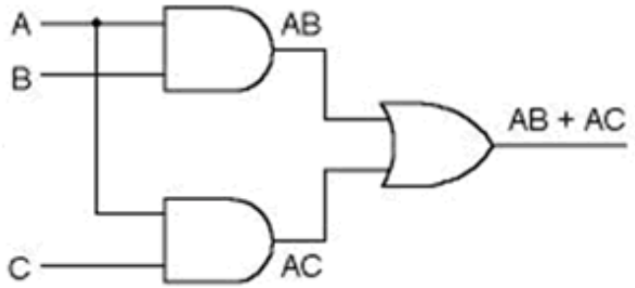


Figure 5: Slice details [2, p. 15].

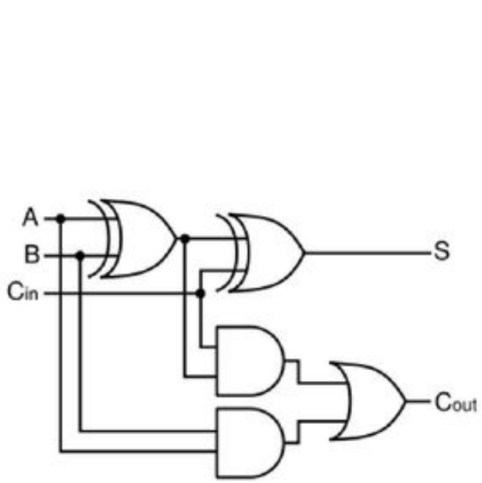
Look-Up Table



A	B	C	AB	AC	AB + AC
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	1	1

Figure 6: Boolean functions with LUTs [4].

Look-Up Table



Truth Table

Inputs			Outputs	
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

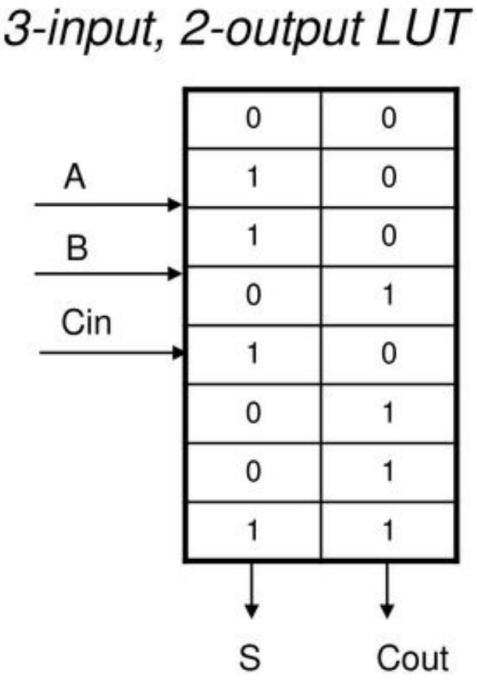


Figure 7: Boolean functions with LUTs [4].

Look-Up Table

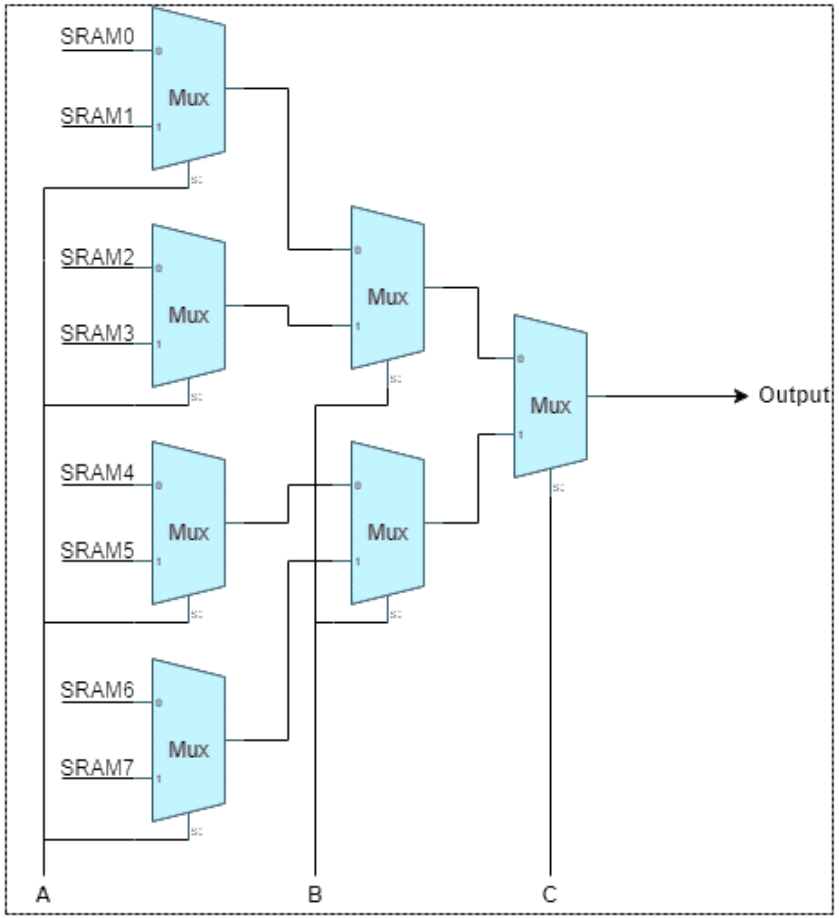


Figure 8: Realization of LUTs [5].

Types of Slices

- $\approx 2/3$: SLICEL logic slices
- $\approx 1/3$: SLICEM logic slices, LUTs also be used as either:
  - Distributed 64×1 RAM
  - 32-bit shift register (SRL32)
  - $2 \times$ 16-bit shift registers (SRL16)

Row Architecture

- Coordinate system numbering
- **X**_ column position (different within CLB)
- **Y**_ row position (same within CLB)

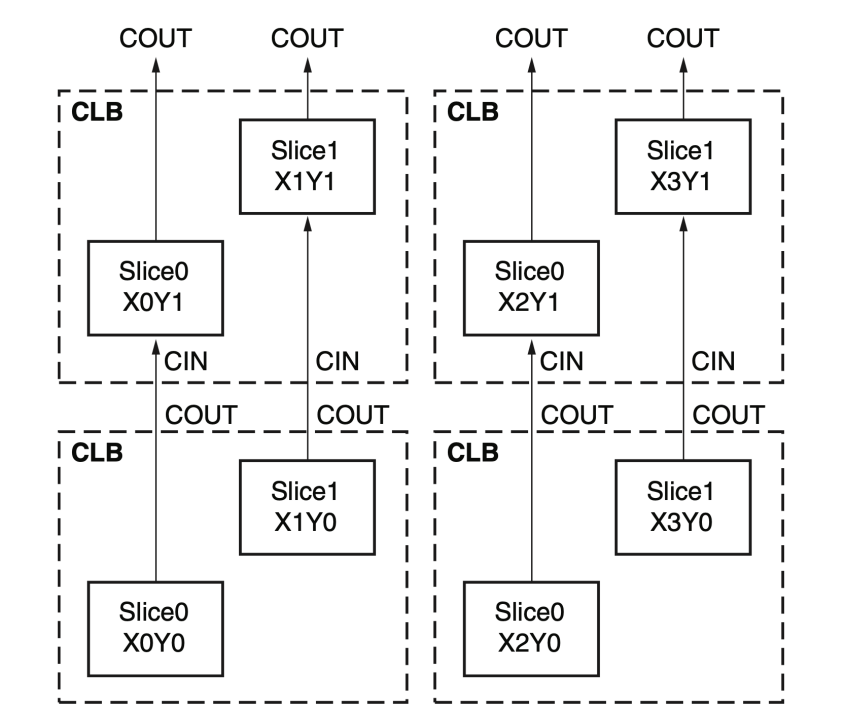


Figure 9: CLB slices [3, p. 17]

Slices in Detail

LUTs

- 6 inputs (`A1` - `A6`)
- 2 outputs (`O5`, `O6`)
- ... for each LUT (`A`, `B`, `C`, `D`)
- Can build
  - any 6-input boolean function
  - 2 $\times$ 5-input boolean functions (common inputs)
  - 2 $\times$ arbitrarily boolean functions with $\{2, 3\}$ inputs or less
- Propagation delay independent of function

Multiplexer

- 3 multiplexer (`F7AMUX`, `F7BMUX`, `F8MUX`)
- `F7AMUX` 7-input function from LUTs A, B
- `F7BMUX` 7-input function from LUTs C, D
- `F8MUX` 8-input function from all LUTs
- Functions with more inputs? Multiple slices

Storage Elements

- 8 storage elements
- 4 $\times$ D-FF (edge) or latch (level)
  - Latch: transparent with CLK is low
- 4 $\times$ only D-FF by LUT (`O5`) or slide inputs
  (only when others are D-FF)
- Control Signals (`CLK`, `CE`, `SR`) shared within slice

Distributed RAM (only SLICEM)

- LUTs can be used as synchronous RAM (DRAM)
- Various options

RAM	Description	Primitive	Number of LUTs
32 x 1S	Single port	RAM32X1S	1
32 x 1D	Dual port	RAM32X1D	2
32 x 2Q	Quad port	RAM32M	4
32 x 6SDP	Simple dual port	RAM32M	4
64 x 1S	Single port	RAM64X1S	1
64 x 1D	Dual port	RAM64X1D	2
64 x 1Q	Quad port	RAM64M	4
64 x 3SDP	Simple dual port	RAM64M	4
128 x 1S	Single port	RAM128X1S	2
128 x 1D	Dual port	RAM128X1D	4
256 x 1S	Single port	RAM256X1S	4

Figure 10: Options for DRAM [3, p. 24].

Shift Register (only SLICEM)

- LUT configurable as 32-bit shift register w/o using FF
- Each LUT can delay data 1-32 clock cylces
- Cascade for larger shift register
- $4 \times$ LUT $=$ 128-bit shift register
- Longer SHR: multiple slices (CLBs)

Interconnect Resources

Interconnect Resources

- Transparent to designers
- Selected types are under user control (e.g., clocking)
- Programmable network of signal pathways
- Connections between: IOBs, CLBs, DSP Slices, BRAM, ...
- CLBs connect to switch matrix
- Connect to general-routing resource
- Vertically / horizontally between CLB rows and columns

Interconnect Resources

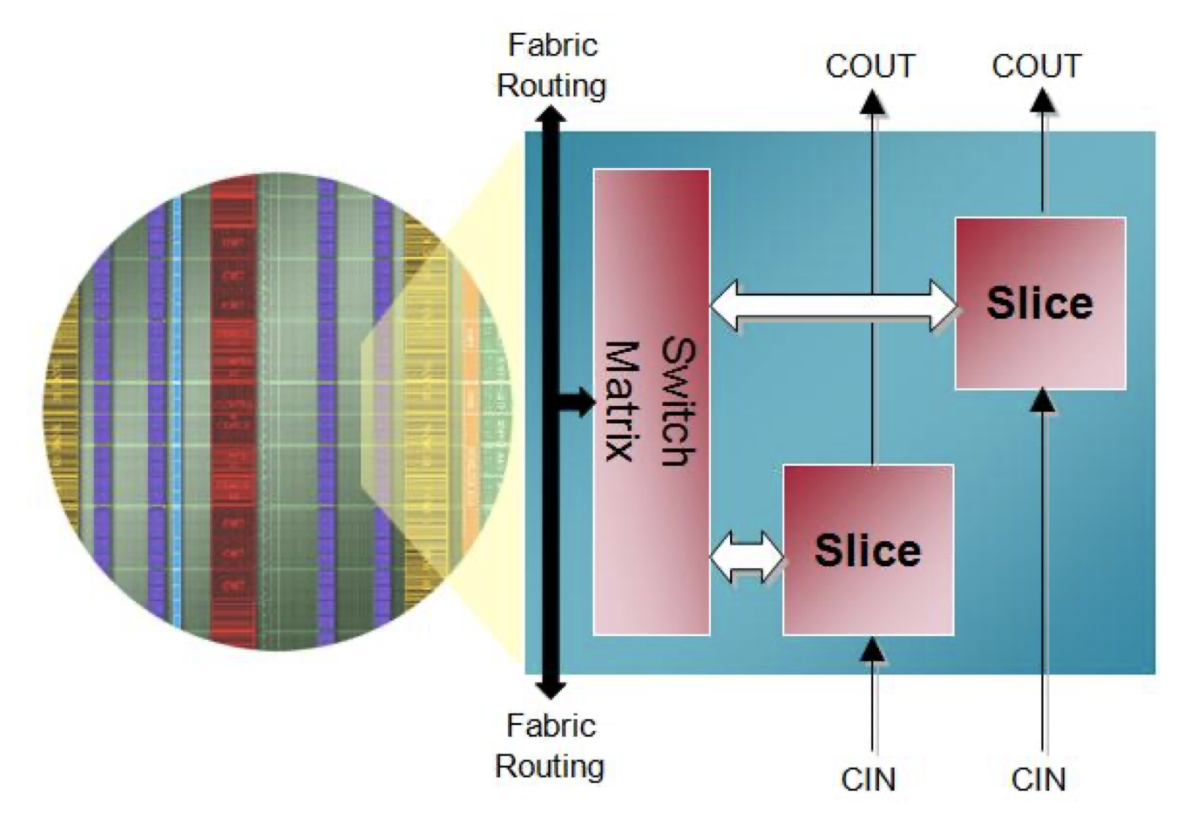


Figure 11: Switch matrix [p. 11, 2].

Interconnect Resources

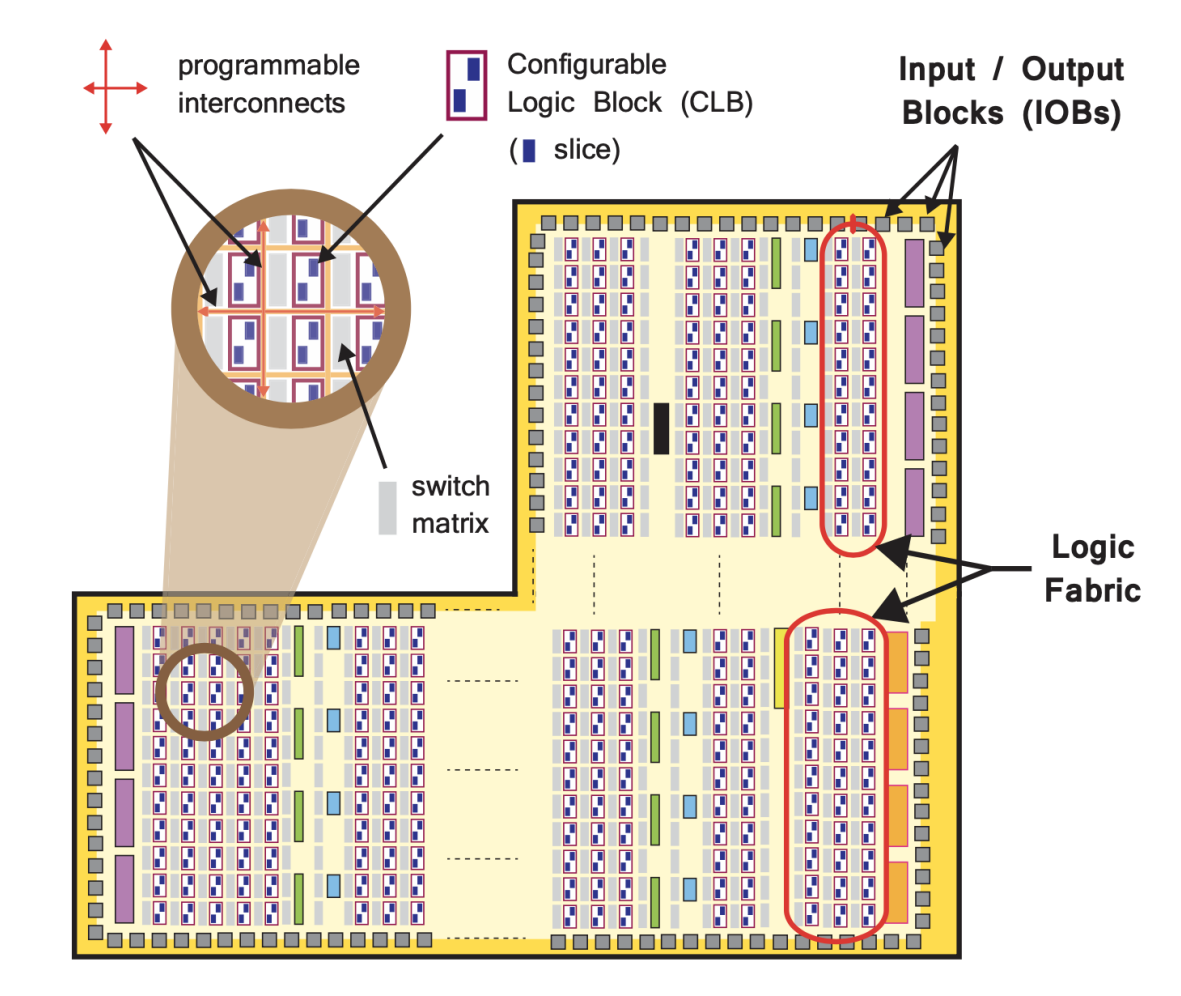


Figure 12: Logic fabric and interconnects [6, p. 23].

SSI (some Virtex-7)

- *Stacked Silicon Interconnect* (SSI)
- In some Virtex-7 devices
- Summarized: a lot of super fast connection to connect super logic regions (SLRs)
- See *CLB User Guide* for more information

SelectIO Resource

SelectIO Resource

- Organized in *banks*
- High performance (HP) banks
  - High-speed memory
  - High-speed chip-to-chip
  - Only up to 1.8V
- High range (HR) banks
  - Wider range of I/O standards
  - Up to 3.3V

I/O Standards

Feature	HP I/O Banks	HR I/O Banks
3.3V I/O standards(1)	N/A	Supported
2.5V I/O standards(1)	N/A	Supported
1.8V I/O standards(1)	Supported	Supported
1.5V I/O standards(1)	Supported	Supported
1.35V I/O standards(1)	Supported	Supported
1.2V I/O standards(1)	Supported	Supported
LVDS signaling	Supported(2)	Supported
24 mA drive option for LVCMOS18 and LVTTL outputs	N/A	Supported
V_{CCAUX_IO} supply rail	Supported	N/A
Digitally-controlled impedance (DCI) and DCI cascading	Supported	N/A
Internal V_{REF}	Supported	Supported

Figure 13: I/O standards, **subset** [7, p. 13].

I/O Banks

- 1 bank = 50 IOBs
  - Pins at edges: single-ended
  - Other 48 pins: single-ended or differential
- input / output / 3-state
- Number of banks defined by device size (pin count)

I/O Block

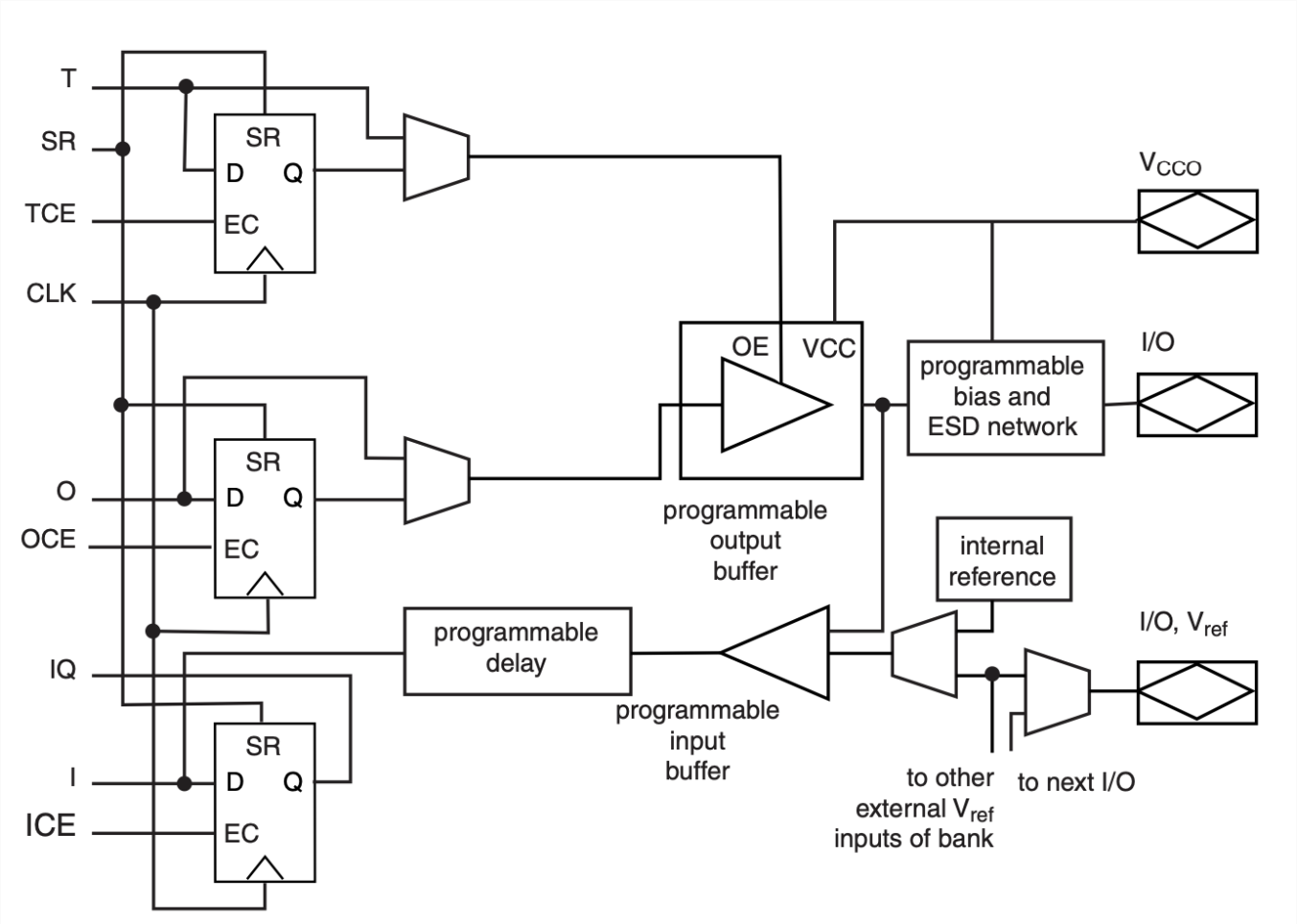


Figure 14: I/O block of Spartan-II [8, p. 140].

I/O Block Components

The usage can be summarized as:

- right side: handling of I/O standards, reference voltage
- left side: buffers, one for I/O/Three-State, FF or latch
- programmable delay: compensate variations in hold time on input path

FPGA Configuration

FPGA Config

- FPGA needs to be configured (volatile)
- Data stored in *CMOS Configuration Latches* (CCL)
- Reprogrammed unlimited number of times
- Different configuration options
  - Master-mode: CLK driven by FPGA
    - (e.g., to load from SPI flash)
  - Slave-mode: FPGA uses CLK input
  - JTAG
- Bitstream length depends on device
  - *7S6* (smallest Spartan): 4,310,752 bits (min 8Mb)
  - *7VH870T* (biggest Virtex): 294,006,336 bits (min 512Mb)

Configuring a 7-series device

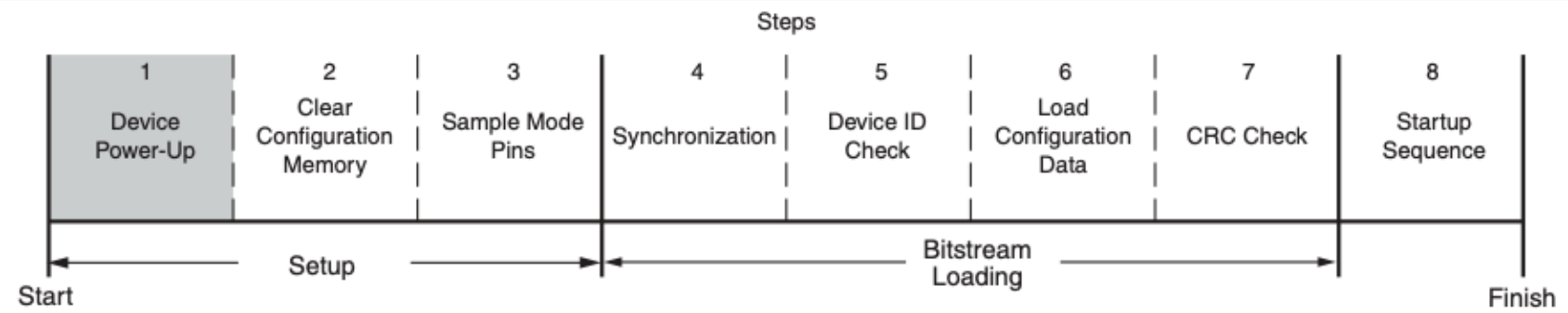


Figure 15: Device power-up [9, p. 85].

Other Resources

RAMB36 Block RAM

- 2×18 Kb or 1×36 Kb
- Various configuration options
  - $64K \times 1$ (with adjacent)
  - $32K \times 1$
  - $16K \times 2$
  - ...
- Synchronous r/w, 2 ports independent
- Data can be initialized by bitstream
- Many, many more configurations

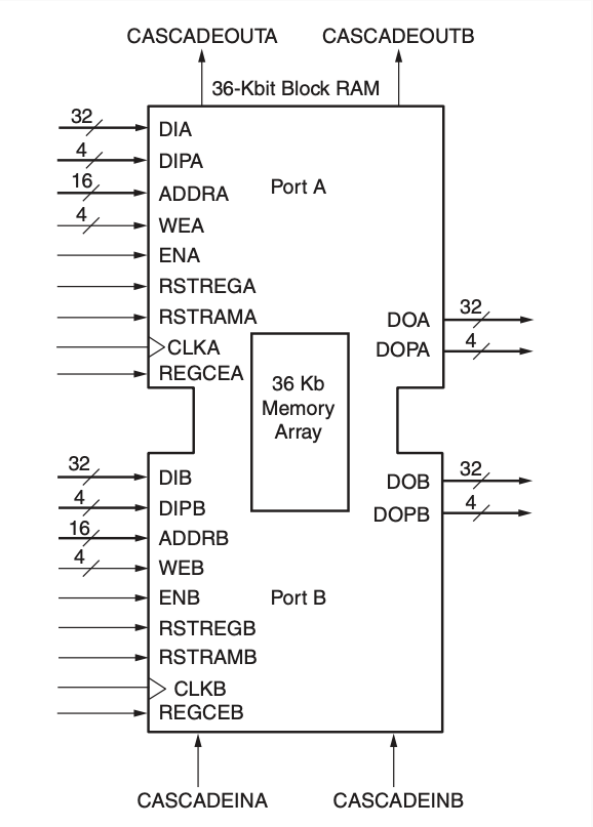


Figure 16: RAMB36 [10, p. 16].

DSP48E1 Slices

- Hardware is great for DSP
- DSP with CLBs is expensive
- Many dedicated, full-custom, low-power DSP slices

DSP48E1 Slices

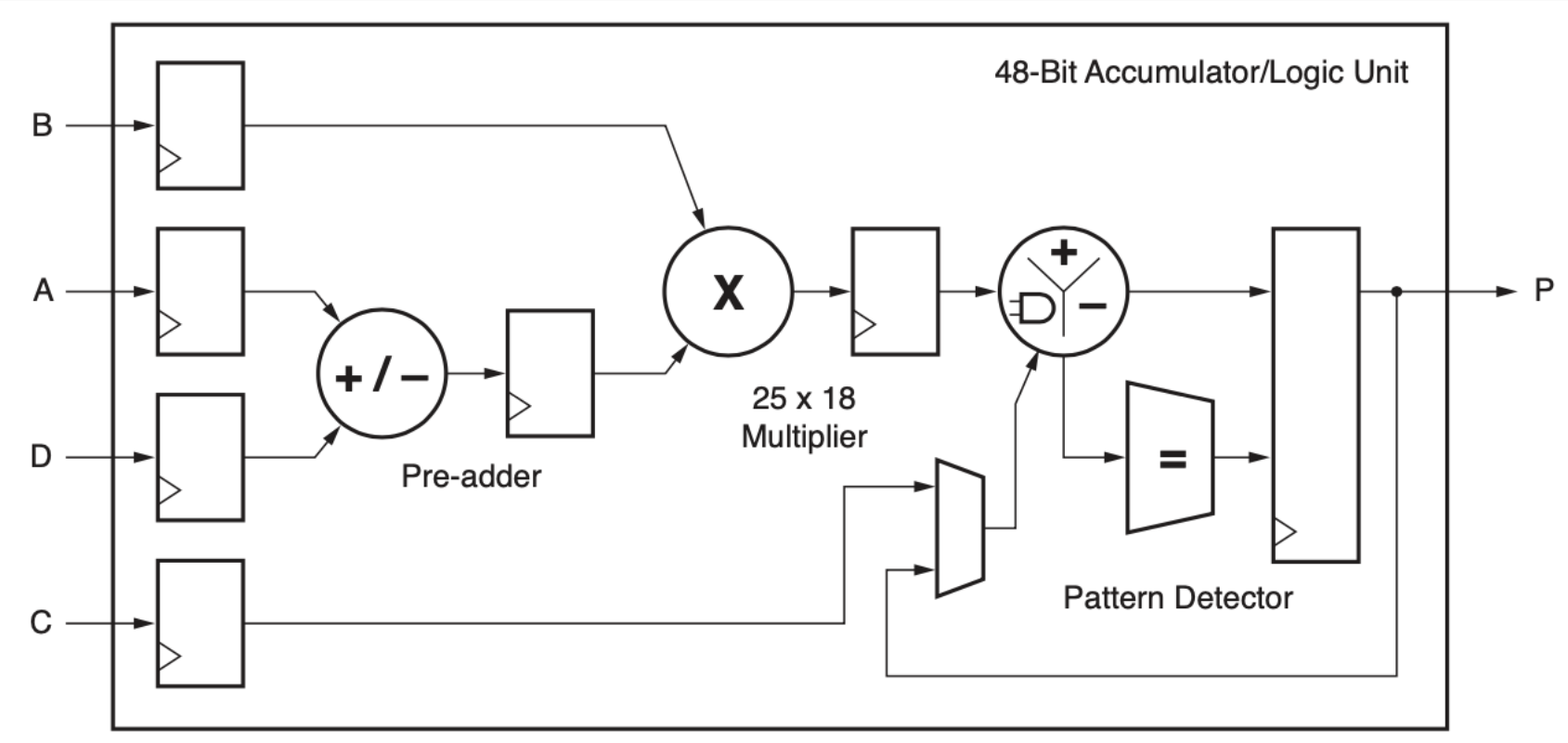


Figure 17: DSP48E1 [11, p. 9].

DSP48E1 Slices

- 25 $\times$ 18 two's complement multiplier
- 48-bit accumulator (opt. sync. up/down counter)
- Pre-adder (for symmetrical filter applications)
- SIMD arithmetic unit (2 $\times$ 24-bit, 4 $\times$ 12-bit)
- Logic unit (any of 10 logic functions of 2 operands)
- Pattern detector (rounding, 96-bit-wide logic function with LU)
- See *7 Series DSP48E1 Slice User Guide* for more details

Clocking

- Clock Management Tiles (CMT) provide frequency synthesis, deskew, jitter filter
- Clock tree to distribute clock signal
- CMTs contain
  - Mixed-Mode Clock Manager (MMCM)
  - Phase-Locked Loop (PLL)
- FPGA divided into clock regions
- More information: *Clocking Resource User Guide*

Thank You For Your Attention

Do you have any Questions?

References i

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[12] Bajaj, Ronak and Fahmy, Suhaib. *Mapping for maximum performance on FPGA DSP blocks* https://www.researchgate.net/publication/282398023_Mapping_for_maximum_performance_on_FPGA_DSP_blocks