Computer Organization and Networks

(INB.06000UF, INB.07001UF)

Chapter 14: Information on the Exam

Winter 2020/2021

Stefan Mangard, www.iaik.tugraz.at

The Written Exams

- All written exams take 90 minutes
- Questions are in English
- You can write your answers in English or German
- Paper and pen only (no calculator, mobile, …) – no red ink, no pencil

Important!

- **Please deregister from an exam immediately, if you decide to not take part in an exam!!!**
- Doing exams during the COVID-19 pandemic is a significant effort for all students and teachers.
- There is no need to add extra effort because of “no-shows”

COVID-19 Regulations

- The exams will take place **on campus**

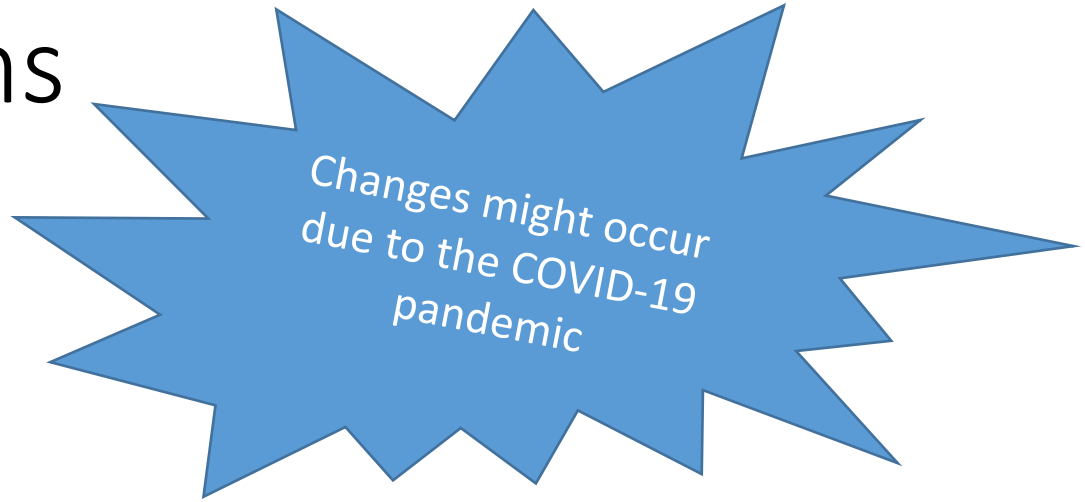
- Read and follow all **COVID-19 regulations** of TU Graz: https://www.tugraz.at/en/studying-and-teaching/international-studying-and-teaching/internationals-at-tu-graz-covid-19-information/#c315783

- Do a **Checkin** to the exam
  - Open the app via checkin.tugraz.at with your smartphone or computer.
  - Use this app to scan the QR code from your assigned seat or at the lecture podium to complete the registration, or you can enter your data manually into the system.
  - If a positive coronavirus case is registered in the direct vicinity of your seat, you will be contacted by TU Graz by e-mail.

  - More information: https://www.tugraz.at/icoe/coronavirus/faq-studierende-students/faq-studienjahr-202021-academic-year-202021/#c350877

- **Do not take part in an exam, if you feel sick**
  (you do not need to bring a confirmation of a doctor – if you can't deregister yourself simply send an email and we will deregister you)

Currently Planned Exams



- 13.02.2021
- 22.02.2021
- Next one is planned to be after Easter
- Next one is planned on 07.06.2021
- There will be no exams during the summer break

General Things

- The exam covers all the content of the lecture including **SystemVerilog** and **RISC-V assembly**

- You are expected to be able to **understand and write** short SystemVerilog and RISC-V assembly statements

- In case of longer assembly examples, we will provide a list of RISC-V instructions with the exam. Example:
  - LW rd,rs1,imm
  - ADDI rd,rs1,imm
  - …

  (no functional description will be provided)

Format of the Exam

- There will be **5 questions** with **10 points** each
  - There will typically be subquestions (a), (b), (c), …
  - Typically there will be 1-2 questions on the network part presented by Johannes Feichtner

- Grading of the exam
  - 45 - 50 pts. → very good (1)
  - 39 - 44 pts. → good (2)
  - 32 - 38 pts. → satisfactory (3)
  - 26 - 31 pts. → sufficient (4)
  - 00 - 25 pts. → insufficient (5)

Example Questions from Previous Years

Finite State Machines

1. (10 points) **Automata:** Given the following truth table of a synchronous automaton consisting of two flip flops (s1, s0), a one-bit input (in), and a two-bit output (out1, out0):
   (a) Show the corresponding ASM diagram of the automaton.
   (b) Show the structural diagram of the automaton featuring logic blocks, flip flops, and wires. Specify the logical formulas for the individual logic blocks.
   (c) Name the type of automaton in this example. What is the name of the second type of automaton and explain the difference between them.

s1	s0	in	out1	out0	next_s1	next_s0
0	0	0	0	0	0	1
0	0	1	0	0	0	1
0	1	0	0	1	1	0
0	1	1	0	1	1	1
1	0	0	1	0	0	1
1	0	1	1	1	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	1

TCP/IP

3. (10 points) **TCP/IP:**
   (a) What is the purpose of MTU Path Discovery?
   (b) How does the standard method work, which protocols are used?
   (c) Why could the standard method fail (and actually does quite often)?
   (d) What is the difference between IPv4 and IPv6 (in relation to MTU Path Discovery)?

Caches

5. (10 points) **Memory and Caches:** Assume a directly-mapped cache with a total size of 64 bytes, organized in 8 blocks, and 256 bytes of byte-addressable main memory.
   (a) Why are caches used in modern processors, *i.e.*, what problem do they solve?
   (b) Name and explain the two types of locality that caches exploit.
   (c) How many bits are needed for addressing the main memory and how many bits of the address are used for tag/index respectively?
   (d) Sketch the directly-mapped cache and explain how a cache access to the address 0x58 is performed. What checks are performed on which data and what are the expected values for a cache hit?
   (e) Sketch a 4-way set-associative cache with the same block size and total size. How many bits are used for tag/index in this configuration? Explain what checks (incl. the expected values) are performed when accessing address 0x58.