CON exam 20.04.2021 Matr.nr.: Last name:

The use of examination aids (e.g., calculators) is prohibited. Answers can be given in German or English. Please refrain from using lead pencils and red ink pens.

Grading scale: 00–25: insufficient 26–31: sufficient 32–38: satisfactory
39–44: good 45–50: very good

Q1. (10 points) **Finite Automaton:** Given the following truth table of a synchronous automaton consisting of two flip flops (s1, s0), a one-bit input (in), and a two-bit output (out1, out0):

(a) Show the corresponding ASM diagram of the automaton.

(b) Show the structural diagram of the automaton featuring logic blocks, flip flops, and wires.

(c) Specify the logical formulas for the individual logic blocks.

(d) Name the type of automaton in this example. What is the name of the second type of automaton and explain the difference between them.

(e) Change exactly three lines of the truth table to create the other type of FSM. The resulting automaton need not be functionally equivalent.

s1	s0	in	out1	out0	next_s1	next_s0
0	0	0	0	0	0	1
0	0	1	0	0	0	1
0	1	0	0	1	1	0
0	1	1	0	1	1	1
1	0	0	1	0	0	1
1	0	1	1	1	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	1

→

→

Q2. (10 points) **Memory and Cache:**

Assume a directly-mapped data cache with a total size of 32 bytes, organized in 4 blocks, and 128 bytes of byte-addressable main memory.

(a) What is a memory hierarchy and why do we need one?

(b) Name and explain the two types of locality that caches exploit.

(c) What is the advantage/disadvantage of a set-associative cache over a directly mapped cache?

(d) Sketch the directly-mapped cache and explain how a cache access to the address 0x56 is performed. What checks are performed on which data and what are the expected values for a cache hit?

(e) What is a replacement policy in the context of caches? Name **2** examples.

Q3. (10 points) **Assembly:**

(a) Explain the RISC-V instructions `JAL` and `JALR` and describe what they do internally in the CPU. What is the difference? Where are these instructions used (provide one application for each of the two instructions)?

(b) Transform the following C-code to RISC-V assembly. All local variables of the C-code **must** be allocated on the stack. The global variable `g` is located at address `0xF00`. The RISC-V calling convention must be followed. The assembly startup code including the initialization of the stack is provided below. Write the assembly code for the two functions at the foreseen locations.

```c
// Located at memory address 0xF00
int g;

int subf(int* p, int t) {
  return *p + t;
}

int main() {
  int a = 7;
  g = 2;
  return subf(&g, a) + a;
}
```

Assembly Reference

```
LW    rd,imm(rs1)
SW    rs1,imm(rs2)
ADD   rd,rs1,rs2
ADDI  rd,rs1,imm
SUB   rd,rs1,rs2
```

```
_start:
  ADDI sp, zero, 0x700
  JAL ra, main
  EBREAK

subf:
```

```
main:
```

Q4. (10 points) **IPv6:**

(a) Why is SLAAC (Stateless Address Auto-Configuratoin) stateless?

(b) What are the four steps of the SLAAC Workflow?

(c) How can one derive an IP address from a MAC address?

(d) Which privacy aspects have to be considered with SLAAC?

Q5. (10 points) **TCP/IP:**

(a) What is the purpose of flow control?

(b) Acknowledging each packet is slow. How can data throughput be increased?

(c) What is the idea of the sliding window mechanism?

(d) Illustrate the principle of sliding window using an example.
(*Hint:* Show what is modified and which protocol parameters play an essential role)

(e) What is the difference between flow and congestion control?

Good Luck!