CON exam 13.02.2021 Matr.nr.: Name:

The use of examination aids (e.g., calculators) is prohibited. Answers can be given in German or English. Please refrain from using lead pencils and red ink pens.

Grading scale: 00–25: insufficient 26–31: sufficient 32–38: satisfactory
39–44: good 45–50: very good

Q1. (10 points) **SystemVerilog FSM:**

(a) Look at the SystemVerilog code and the incomplete timing diagram below. Complete the missing signals in the diagram. Use binary encoding for signal values.

(b) Draw the ASM diagram for this finite-state machine.

(c) Draw the output logic as gate-level netlist.

(d) What kind of finite-state machine is given? What is the name of the other type of finite-state machines? Explain the difference between the two types of finite-state machines.

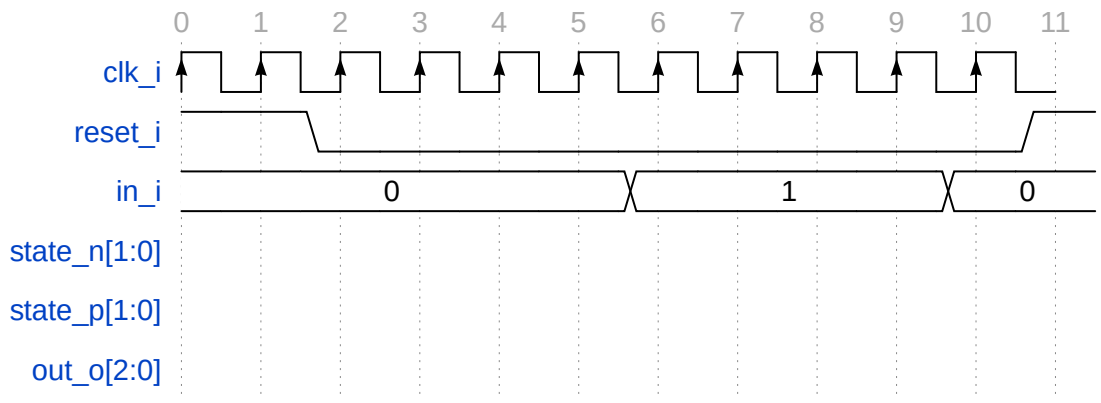
(e) Change the SystemVerilog code to create a finite-state machine of the other type. The functionality of the new FSM may be different than the one of the given FSM.

```
module state_machine(
  input logic clk_i,
  input logic reset_i,
  input logic in_i,
  output logic [2:0] out_o
);
  logic [1:0] state_p, state_n;

  always_ff @(posedge clk_i or posedge reset_i) begin
    if (reset_i) state_p <= 2'b00;
    else         state_p <= state_n;
  end

  always_comb begin
    if (in_i == 0)
      state_n = state_p + 1;
    else begin
      case (state_p)
        2'b00:   state_n = 2;
        2'b01:   state_n = 3;
        2'b10:   state_n = 1;
        default: state_n = 0;
      endcase
    end
  end

  always_comb begin
    out_o[0] = 1;
    out_o[1] = state_p[0] | state_p[1];
    out_o[2] = state_p[0] & state_p[1];
  end
endmodule
```



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Q2. (10 points) **Pipelining:**

(a) Explain the motivation and concept of pipelining based on the following example. You have a single cycle machine with a critical path of 600ps. You are able split the path into three pipeline stages of 200ps each. What does it mean to insert a pipeline stage? Explain how this leads to a speedup. How much is the speedup (assuming a full and ideal pipeline)?

(b) Assume the three pipeline stages `IF`, `ID` (includes reading the operands from the register file), and `EX`. This pipeline executes the three instructions below. Explain the problem arising in the pipeline with this code snippet. Explain two approaches to resolve this problem.

(c) Complete the diagrams below for both approaches and show which pipeline operation is performed at what clock cycle for each instruction of the code snippet. Assume an empty pipeline before starting the execution. State the total number of needed clock cycles for the execution of the code snippet for both approaches.

(d) Motivate the need of a reorder buffer and explain its basic concept.

```
ADDI x2, x1, 0  # I1
ADDI x3, x1, 5  # I2
ADDI x4, x3, 3  # I3
```

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Q3. (10 points) **Assembly:**

(a) Explain the RISC-V instructions `JAL` and `JALR` and describe what they do internally in the CPU. What is the difference? Where are these instructions used (provide one application for each of the two instructions)?

(b) Transform the following C-code to RISC-V assembly. All local variables of the C-code **must** be allocated on the stack. The RISC-V calling convention must be followed. The assembly startup code including the initialization of the stack is provided below. Write the assembly code for the two functions at the foreseen locations.

```
int times3(int* p) {
  return *p * 3;
}

int main() {
  int a = 3;
  return a + times3(&a);
}
```

Assembly Reference

```
LW    rd,imm(rs1)
SW    rs1,imm(rs2)
ADD   rd,rs1,rs2
ADDI  rd,rs1,imm
SUB   rd,rs1,rs2
```

```
_start:
  ADDI sp, zero, 0x700
  JAL ra, main
  EBREAK

times3:
```

```
main:
```

Q4. (10 points) **ARP:**

(a) Why is it needed?

(b) What kind of messages are sent with ARP? Describe their technical structure.

(c) What is the idea behind Gratuitous ARP messages? How is their structure different to regular messages?

Q5. (10 points) **TCP/IP:**

(a) What is the purpose of MTU Path Discovery?

(b) How does MTU Path Discovery work, which protocols are used?

(c) Why could MTU Path Discovery fail (and actually does quite often)?

(d) What is the difference between IPv4 and IPv6 regarding MTU Path Discovery?

Good Luck!